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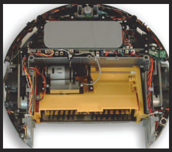

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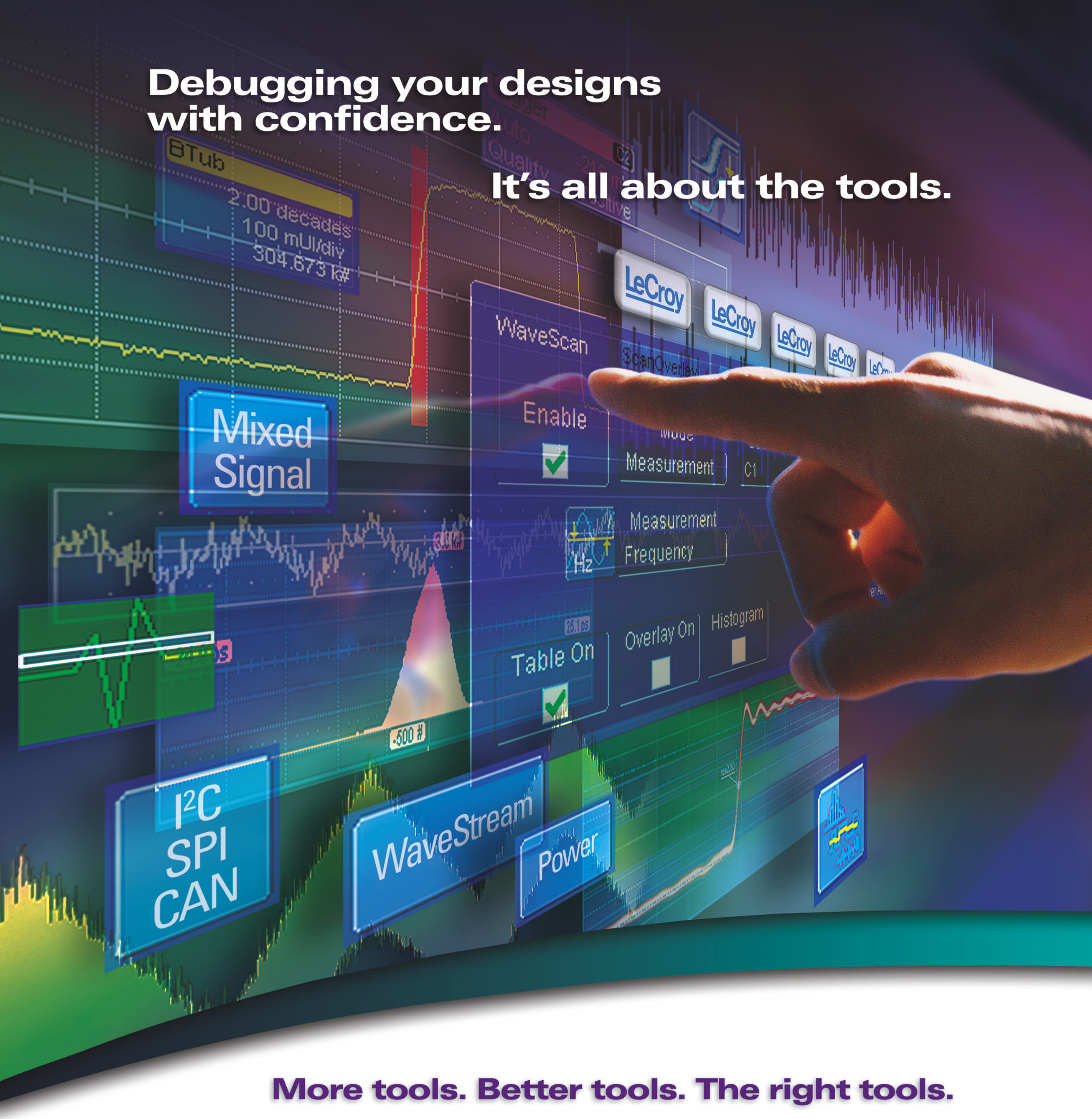
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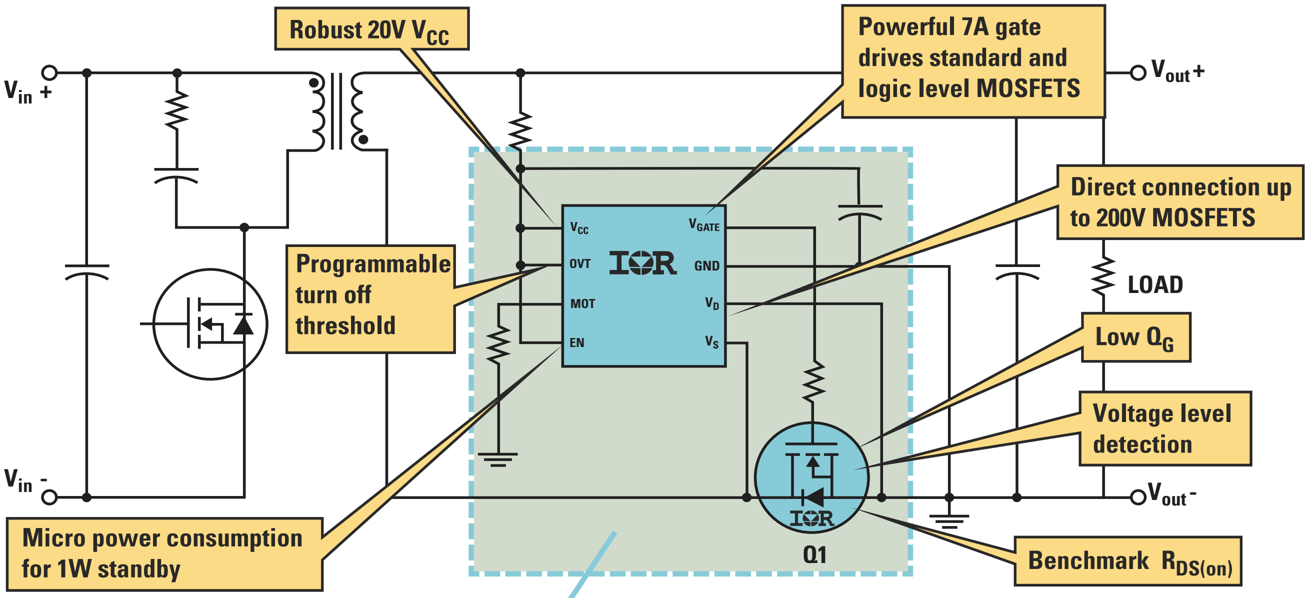

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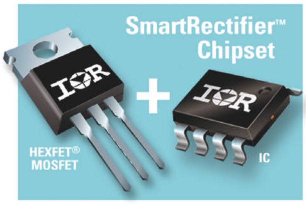

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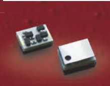

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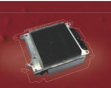

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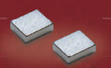

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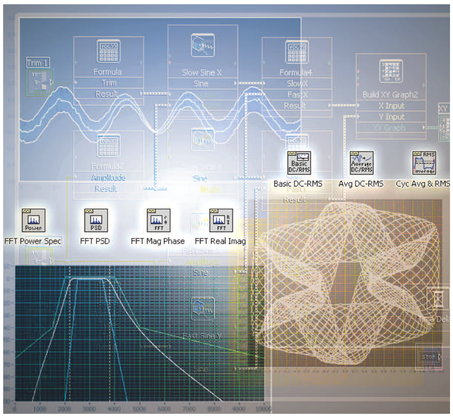

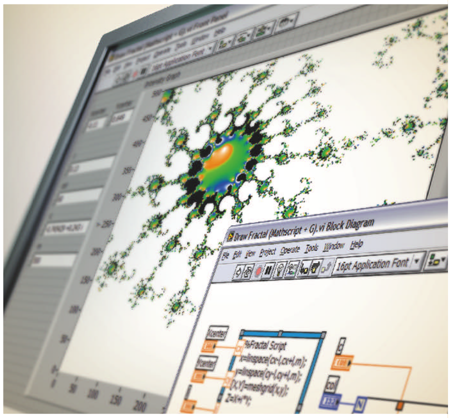

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Choosing to use an SIP

63 Developing an SIP product rather than an SOC for a portable multimedia platform begins with careful architecture planning.

by Mario Manninger, austriamicrosystems

Board standards seek the holy grail

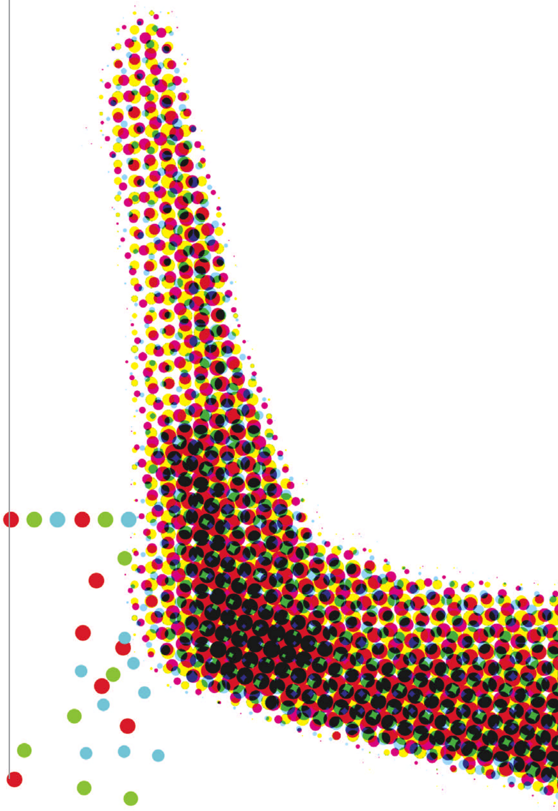
50 As expectations for embedded systems soar, standards organizations are scrambling to offer designers the best combination of cost, size, reliability, and performance.

by Warren Webb, Technical Editor

Imaging beyond pixels: enhancing the elementary picture

35 With per-sensor pixel growth slowing, how else can digital-still-camera manufacturers differentiate from each other? How does this differentiation bring them into greater competition with videocameras? To what degree will camera phones supplant them both? And where will sensor suppliers turn to continue filling their fabs?

by Brian Dipert, Senior Technical Editor



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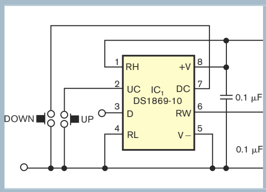

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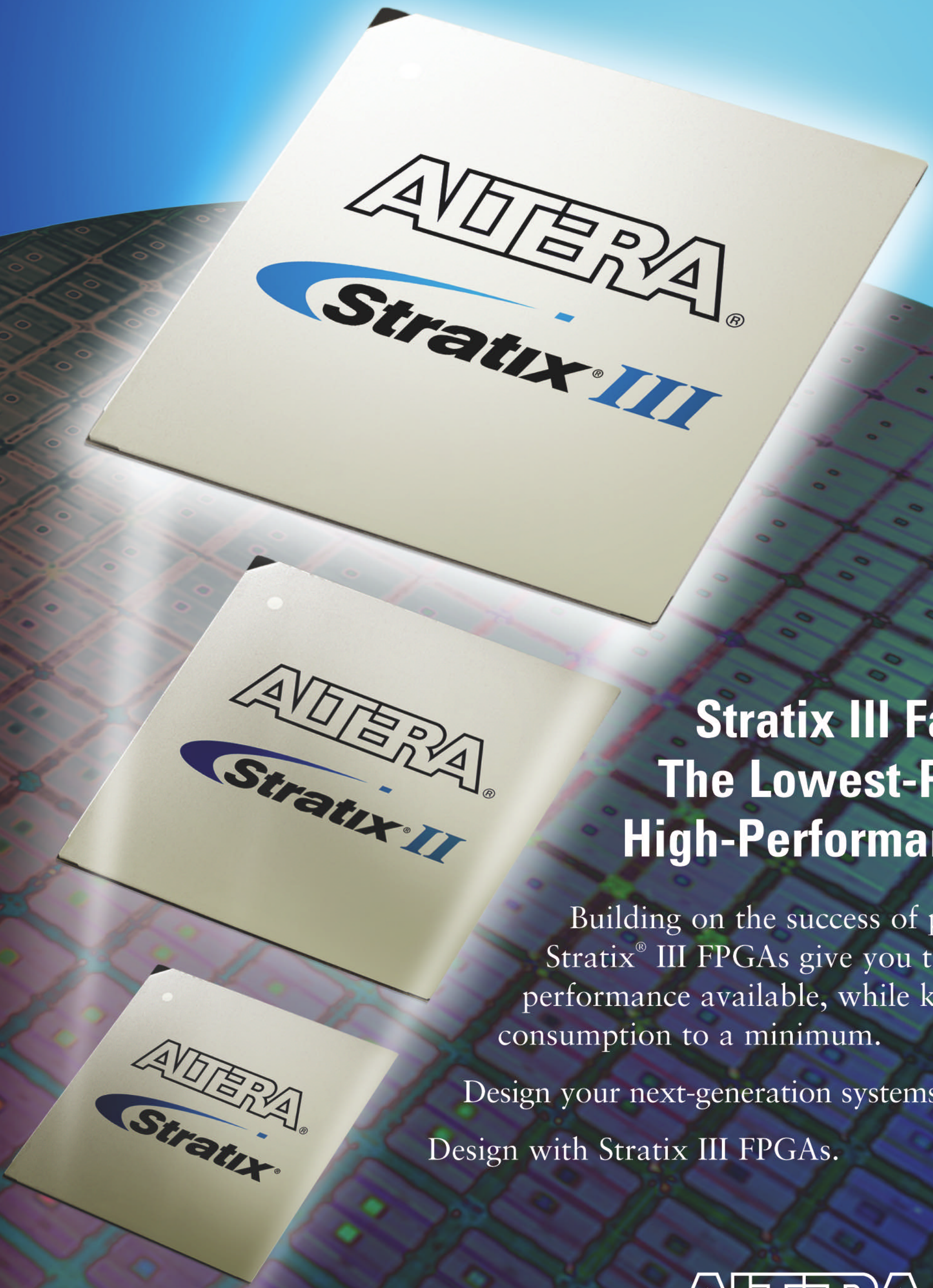

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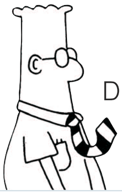

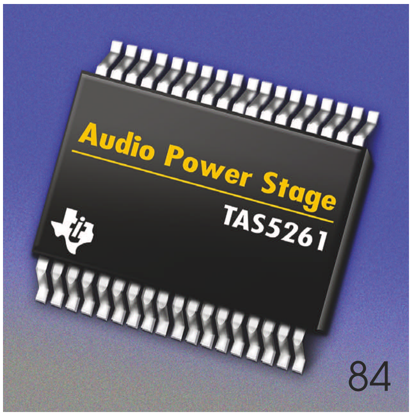

DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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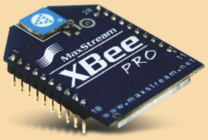

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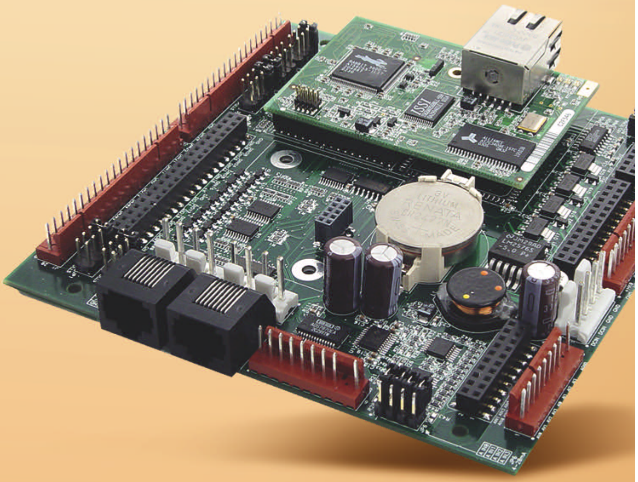

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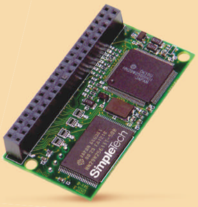

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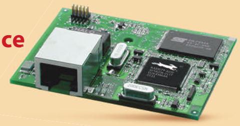

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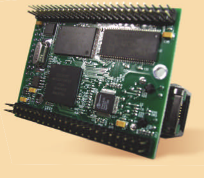

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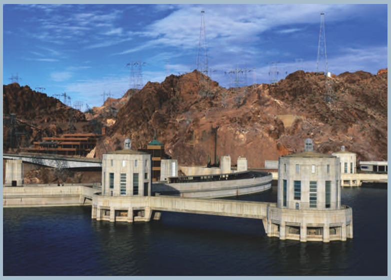

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DRAM interfaces for media-rich SOCs: Searching architectures for bandwidth
DRAM bandwidth and latency have become the most critical issues in the design of media-processing chips, and they appear also to be the issues least susceptible to easy fixes.
→www.edn.com/article/CA6417194

Linux on the PS3: A hit, albeit with a few strikes
Sony officially blesses alternative operating systems on the PS3. I chose to install Yellow Dog Linux.
→www.edn.com/070315t2

RapidIO challenges Ethernet
Warren Webb points to a RapidIO white paper that exposes many technical details useful for either RapidIO or Ethernet in embedded applications.
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MP3 patents: Just a symptom of the problem
The recent court decision against Microsoft in the suit over fundamental MP3 patents is yet another indication that the international patent system is rapidly collapsing.
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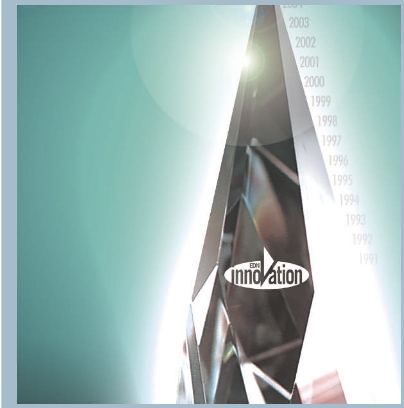

INNOVATION AWARDS

The votes are in. Now comes the fun part. Please join *EDN* April 2 in San Jose, CA, as we proudly present the 17th Annual Innovation Awards. Use the URL below to review the finalists, get event details, and buy your tickets.
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BY MAURY WRIGHT, EDITOR IN CHIEF

China assembles today, innovates tomorrow

Not another piece about China, right? I suspect that's your first thought, but please stay with me. I'm writing this while attending the Globalpress Electronics Summit 2007, and last night, we heard from an untraditional—at least at a tech conference—speaker. Renowned economist Henry Rowen gave a talk on China that stayed away from hype yet recognized the potential of a sleeping giant.

Rowen is a senior fellow at Stanford University's Hoover Institution (www.hoover.org) and a professor emeritus at Stanford's business school. He's served on a presidential commission and happens to be the father of Tensilica Chief Executive Officer Chris Rowen, and *that's* how he came to speak at the conference.

Early on, Rowen stated, "China is an assembler, not an end-to-end manufacturer of products." He noted that it's still primarily Taiwanese companies that manage the process and control the end products. Rowen also noted that China today isn't a huge consumer of goods—at least not on the scale of the hype in the press. He quipped, "Air freight across the Pacific must be a really good business."

But Rowen wasn't suggesting that anyone underestimate the potential of China as a world-class competitor or consumer. He pointed out that the likes of Yahoo and eBay have failed to penetrate the market in China, beat out by local Internet-services companies. Both government assistance and the fact that the local companies know the market presumably hampered the North American brands.

> **Rowen noted that China today isn't a huge consumer of goods—at least not on the scale of the hype in the press.**

Rowen broadly claims that, in the tech industry, China is doing almost no R&D. But he does claim that China is doing significant design work. He pointed out that 10 years ago, China ranked 57th on the list of countries that won the most patents. According to Rowen, China had moved to the 18th spot two years ago. Now, 18th is still fairly far down in the overall scheme of things, but the forward direction is clear.

As for the level of innovation, Rowen said, "The Chinese government finds this deeply unsatisfactory." But Rowen argued that the Chinese industry has done exactly the right thing: finding the low-hanging fruit and taking advantage of innovation from North America, Europe, and Japan. He claimed that 200 years ago, the United States did exactly the same thing: taking advantage of technology from Europe without paying royalties. Later, *EDN* Executive Editor Ron Wilson argued that the analogy was a bit off, as the British refused to share technology with the newly established United States, but clearly, the colonies originally depended on borrowed innovation. On China's attitude toward royalties, Rowen quipped, "I think it doesn't like paying royalties to Qualcomm."

China is certainly escalating R&D investments. Rowen claimed that such spending totaled $30 billion in 2005, but that total is slated to reach $200 billion by 2020. He also stated, "China has the most competent economic management in the world." Now, he also implied that the government hasn't been nearly so competent in developing the tech industry.

Discussing the speech, *EDN*'s Wilson questioned whether you can compare what happened in the development of North America with what is happening in China because of cultural differences. I don't think anyone can know. The question remains as to whether China will play within the bounds of the intellectual-property rules prevalent in North America, Europe, and Japan.

In closing, Rowen was both optimistic and cautionary. On the escalating investments China is making, he claimed that the world market is expanding and that such expansion is a good thing. But he also said, "Maybe a Chinese hedge fund someday will try to scarf up Texas Instruments or Nokia."**EDN**

Contact me at mgwright@edn.com.

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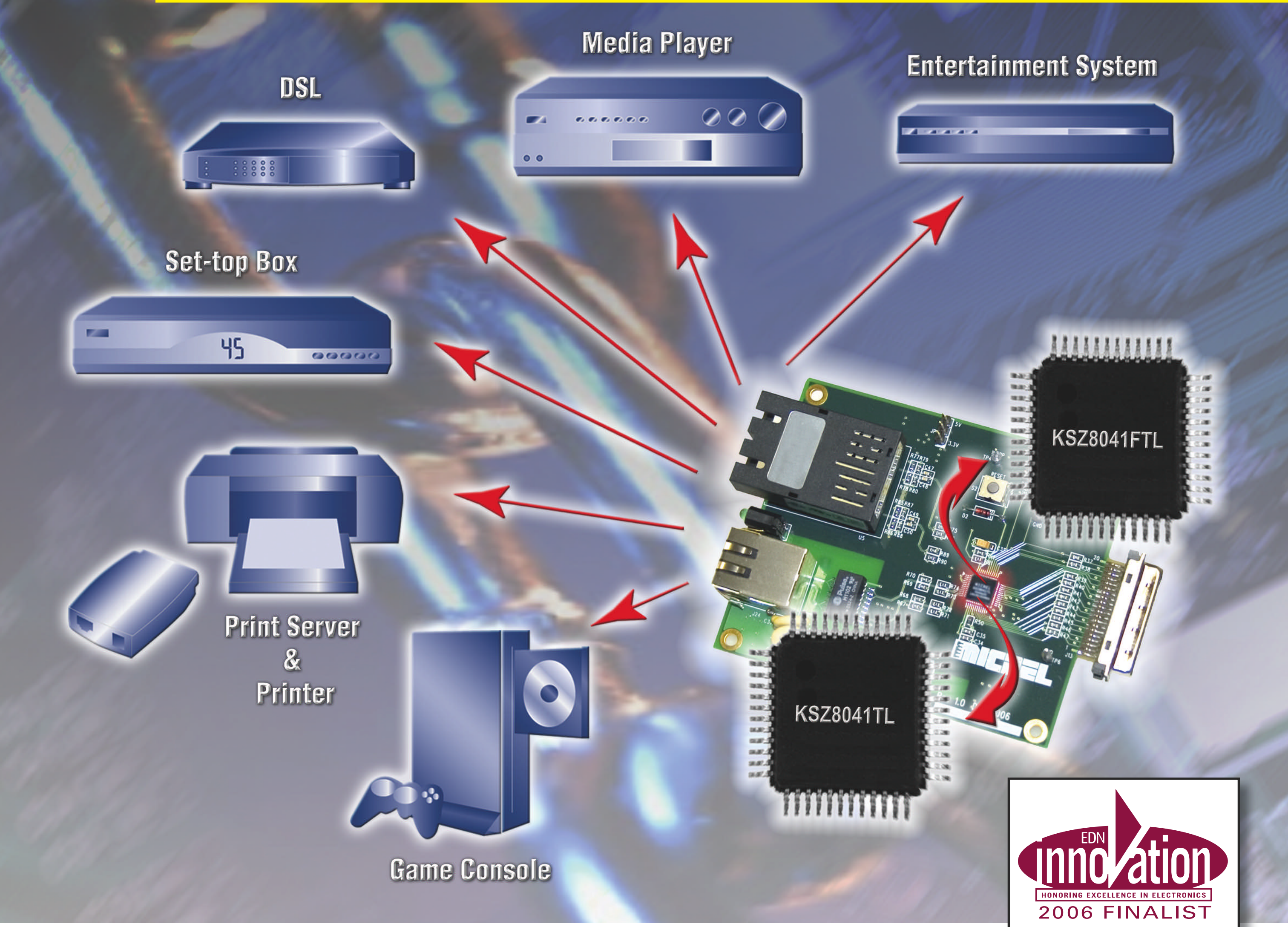

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Reed Electronics Group

ANALOG edge℠

Simplify CCD/CIS Image Capturing with a 3-Channel 16-Bit AFE/Timing Generator

Application Note AN-1583

Robert LeBoeuf and Joseph Clark, Applications Engineers

When designing equipment that deals with amplifying and processing delicate signals, engineers are often faced with the decision of what to mount close to the source, and what can exist further away. These are typically sources like antennas and high impedance audio/video sources. Constraints are more severe with mechanical motion or space. National's LM98714 3-channel, 45 MSPS Analog Front End (AFE) with integrated CCD timing generator and LVDS/CMOS outputs addresses many of these issues.

Multi-Function Peripherals

Multi Function Peripherals (MFPs) are relatively small image copy, scan, and print devices found in thousands of home desktop settings. Historically, these devices have had modest reproduction speeds (gauged in pages per minute) and offered the home user an inexpensive solution to document reproduction. With the speeds of MFPs increasing rapidly, more businesses are finding the MFP satisfies many office tasks once only practical with high speed, industrial-sized digital copiers. The increase in MFP performance comes with new design challenges for the system level architect.

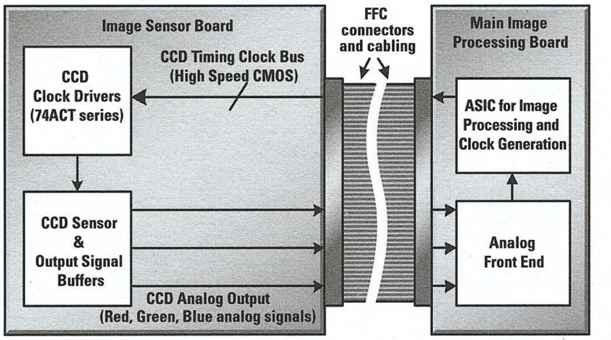

Figure 1. Legacy MFP Image Sensor Block Diagram

Engineers designing copiers and scanners are often faced with mechanical and electrical constraints which challenge the system-level budget. The heart of any copier, whether it is a low-cost MFP or high-performance office model, is the image sensor board whose main component is the Charge Coupled Device (CCD) or Contact Image Sensor (CIS). In older MFP applications, as depicted in *Figure 1*, the image sensor board receives high speed CMOS timing clocks to drive the CCD and sends sensitive analog pixel data to the AFE on the image processing board.

As the speed requirements of the MFP market increase, the system level partitioning shown in ***Figure 1*** exposes new problems. Among the major concerns are increased EMI emissions from high-speed CMOS data traveling across long cables (several hundred mm in most cases) and degraded analog performance. The LM98714 facilitates a breakthrough in system-level partitioning that addresses these concerns.

Analog Front Ends

The LM98714 is an extremely versatile Analog Front End (AFE) with a fully programmable CCD Timing Generator capable of clocking most any sensor. The ADC Data Outputs can be programmed for CMOS levels for legacy designs or slower speed applications (typically <30 MSPS). More importantly, it can also be configured as serialized LVDS for reliable 45 MSPS data transmission. The combination of the full feature AFE, CCD Timing Generator, and LVDS outputs allow the merging of the analog signals onto one board, which eliminates most of the high-speed CMOS digital signaling on the cable.

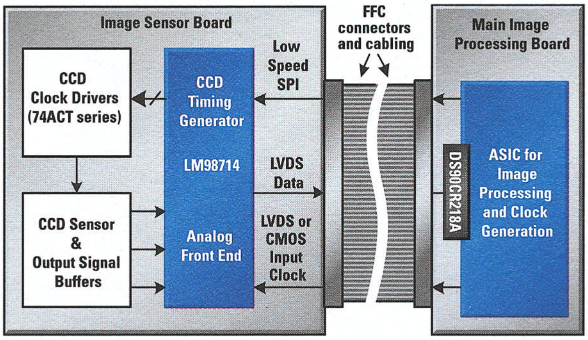

Figure 2. New MFP Image Sensor Block Diagram Partitioning

The LVDS output data can be deserialized by the ASIC, or by using one of National's LVDS Channel Link receivers, such as the DS90CR218A as shown in ***Figure 2***.

National Semiconductor
The Sight & Sound of Information

In addition to the EMI reduction when using LVDS outputs, the LM98714 allows the use of an LVDS input clock. To achieve an even further reduction in EMI, the input clock can be sent to the LM98714 at the pixel rate instead of the full sampling rate.

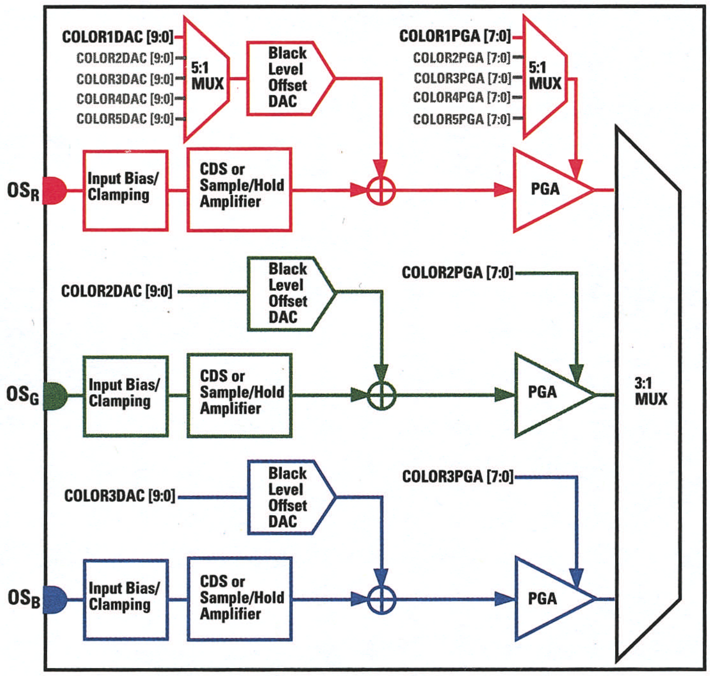

Figure 3. LM98714 Input Diagram

For example, if the CCD has three channels of color per pixel (i.e. Red, Green, and Blue), the LM98714's internal A/D Converter (ADC) runs at 3x the incoming pixel rate. At the maximum sample rate of 45 MSPS, the input clock to the LM98714 can be set to 15 MHz (pixel rate), or 45 MHz (ADC rate). A simple configuration register change via the SPI of the LM98714 makes this feature readily available by applying a multiplication factor to the input clock (3x or 1x respectively). The only remaining non-LVDS signals on the cable with this new architecture are in the SPI interface. The SPI can be run at very low frequencies if found to be a source of significant EMI.

The CCD is a linear image sensor with three color arrays (red, green, and blue) of 10680 elements and an additional array for black-and-white image captures.

In 3-channel mode, OSB, OSG, and OSR are sampled synchronously at the pixel rate. The sampled signals are processed with each channel's offset and gain adjusted independently via the control registers. The order in which pixels are processed from the input to the ADC is fully programmable and is synchronized by the SH pulse. The signals are then routed through a 3-1 MUX to the ADC. *Figure 3* shows a diagram of the channels, and how they are conditioned before the MUX.

The 3 RGB signals are inputted from the left and enter the input bias and clamping block. After the signal is sampled via Sample and Hold or CDS, a unique black offset may be added to each color. This signal may now be gained in the analog domain using the PGAs shown. The MUX now switching at 3 times the pixel rate sends the RGB signals to the ADC to be digitized.

The LM98714 is a fully integrated, high performance 16-bit, 45 MSPS signal processing solution with a maximum input level of 1.2 or 2.4V modes (both with + or – polarity option). Other key specifications include: INL +/- 23 LSB (typ), SNR -74 dB at 0 dB PGA gain, 15/22.5/30 MSPS channel sampling rate, 256 PGA gain steps, and a PGA gain range of 0.7 or 7.84x. The power dissipation is 505 mW (LVDS) and 610 mW (CMOS).

The feature set of the LM98714 is too large to encompass in this article, however, this is one example of its application. Powerful features, such as an analog front end timing generator (used to adjust the sampling points of the analog inputs) and the automatic black level calibration loops are a few of the additional benefits included in the LM98714 architecture. ■

For Additional Design Information

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The Sight & Sound of Information

EDITED BY FRAN GRANVILLE

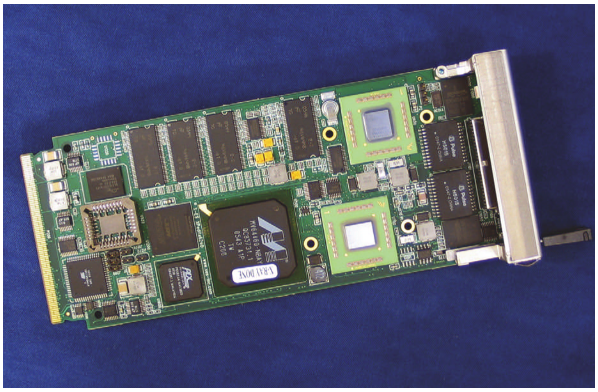
pulse

INNOVATIONS & INNOVATORS

Board computer boosts performance, cuts power

Extreme Engineering Solutions has recently introduced a 3U single-board computer featuring the latest low-power, dual-core PowerPC processor from PA Semi (www.pasemi.com). The XPedite8070 targets the growing requirement for higher performance CPUs for the most sophisticated avionics, radar, software-defined radio, unmanned aerial vehicles, and similar applications. The company based the XPedite8070 on the VITA (VMEbus International Trade Association) VPX-REDI (Ruggedized Enhanced Design Implementation) form factor. Its onboard features include a 1-Gbyte DDR 2 memory for each processor core; a 1-Gbyte NAND flash; and PCI Express, XAUI (10-Gbit-attachment-unit interface)-Ethernet-fabric-interconnect, dual SGMII (serial-gigabit media-independent-interface), and dual isolated gigabit-Ethernet ports. The board typically dissipates 34W at a 1.5-GHz clock speed, and it can run at lower speeds in lower power applications.

Extreme Engineering provides software support for Linux, Wind River's (www.windriver.com) VxWorks, and Platform for Network Equipment Version 1.4. Prices for XPedite8070 start at $7800 (one), and OEM prices approach $5000, depending on volume, memory, and processor configurations. A companion desktop-development chassis is available for $2000.**—by Warren Webb**
▷**Extreme Engineering Solutions**, www.xes-inc.com.



The XPedite8070 with its dual-core PA6T-1682 processor extends the performance-per-watt envelope in the VPX-REDI market.

Jeda offers SystemC-assertion-coverage tool

Privately held EDA company Jeda Technologies has added the NSCv (native-SystemC-verification) tool to its SystemC-tool suite. Last year, the company introduced its NSCa (native-SystemC-assertion) tool to give C++-savvy architects an easier way to create assertions for SystemC using a C++ environment (see "Jeda offers ESL-assertion tool," *EDN*, Feb 21, 2006, www.edn.com/article/CA6309146).

With NSCv, the company helps users ensure that the SystemC code they are creating is functionally thorough. NSCv primarily targets the improvement of verification environments for users of Cadence's (www.cadence.com) SCV (SystemC Verification) testbench-generation tool, although users of competing testbench-generation tools can also use NSCv.

"There are no comprehensive verification solutions out there for SystemC," says Stephen Pollock, Jeda's vice president of marketing. "Most offerings are simulation-based, and those that are testbench-based still need to mature. We're adding new functions to these flows and filling in areas where they are weak."

The tool brings range, cross, transition, and group coverage to SystemC-verification environments. The range coverage measures whether the code covers a range of values for a group of signals. The cross-coverage feature measures the cross coverage of two vectors. Architects use the transition coverage primarily for state-machine verification to measure whether the code covers legal and illegal paths, and the group-coverage feature measures the coverage for a group of coverage points. Prices for NSCv starts at $15,000 for a one-year subscription.

—by Michael Santarini
▷**Jeda Technologies**, www.jedatechnologies.com.

Stream Processors aims at parallel-signal processing

Start-up SPI (Stream Processors Inc) has unveiled a DSP architecture for tackling high-performance, massively parallel-signal processing without requiring designers to learn a new and esoteric software-development model. The processor architecture relies on two MIPS (www.mips.com) 4KEc processor cores in conjunction with a DPU (data-parallel unit) that consists of a scalable number, currently eight or 16, of processing lanes. The system processor, a 4KEc core, runs the application operating system and software, and it manages the system I/O. The other MIPS core and the DPU make up the DSP-coprocessor subsystem. The MIPS core communicates with the DSP dispatcher that manages the runtime synchronization of instructions and DMA data loads for the kernel functions that will execute in the DPU.

The multilane DPU architecture executes the same VLIW (very-long-instruction-word) instructions across all the lanes. Each lane includes five 32-bit ALUs (arithmetic-logic units), including MAC (multiply/accumulate) units, four LRF (lane-register-file) load/store units, and a COM unit for interlane communication. Each ALU in the lane is independent and operates on local data.

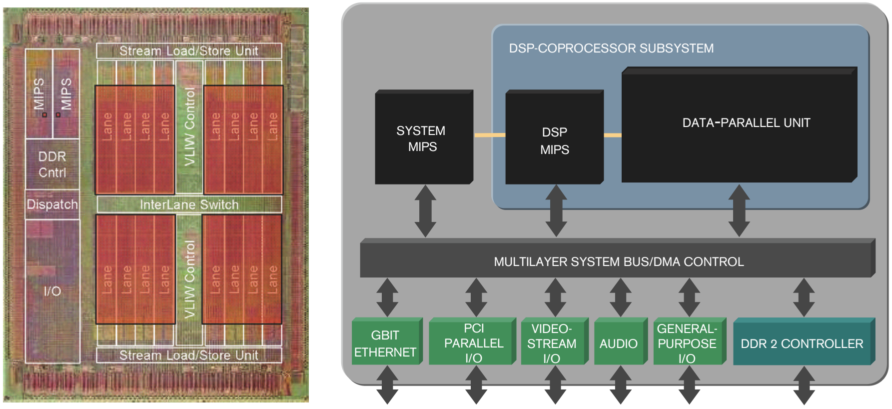
This processing architecture best suits applications that are heavily computationally intensive on streaming parallel data. One of SPI's processors can encode high-definition 1080p video (H.264 HD) in real time and still perform custom video enhancements, image tuning, and content analysis. Because the target applications are streaming data in nature, the system has no conventional cache. Instead, the compiler allocates the data into each device lane through an operand-register-file hierarchy. The same kernel function executes across all of the lanes, with each lane operating on a unique set of data. A high-speed interlane switch supports data exchange across all of the lanes.

The SPI compiler can support and exploit a C-programming model without special parallel constructs. After a designer explicitly marks the beginning and end of the computationally intensive kernel functions and the associated input and output data streams with intrinsics, the compiler implements static-flow analysis to effectively unwrap loops and optimize the on-chip-memory allocation to best use the local memories in each processing lane. By allowing the compiler to implement the parallelism from the C source, the source code remains compatible with chips with different numbers of lanes.

Both devices are available for sampling now, and high-volume-production support is scheduled for July of this year. The 16-lane SP16-G160 is available for $99 (10,000), and the eight-lane SP8-G80 is available for $59 (10,000). The Storm-1 development kit is available now with a BSP (board-support package), printed documentation, and sample applications. The Eclipse-based RapiDev development environment includes the SPC compiler for the Storm-1 family; a cycle-accurate TCS (target-code simulator), including MIPSsim; and FFD (fast-functional-debugger) host-simulation libraries. The development-environment operating-system support includes Linux user-package distribution for SP16 as well as the Linux Kernel (2.6.12) and drivers for SP16, and it includes cross compilers for Linux (Red Hat Enterprise Linux 3, Fedora Core 5) and Windows XP. The development board in the development kit includes a Storm-1 SP16 with 512 Mbytes of SDRAM and 32 Mbytes of flash memory, a PC-compatible PCI-edge connector, an image-sensor connector, 10/100/1000-Gbit Ethernet, analog-audio in/out, and a power supply for stand-alone operation.

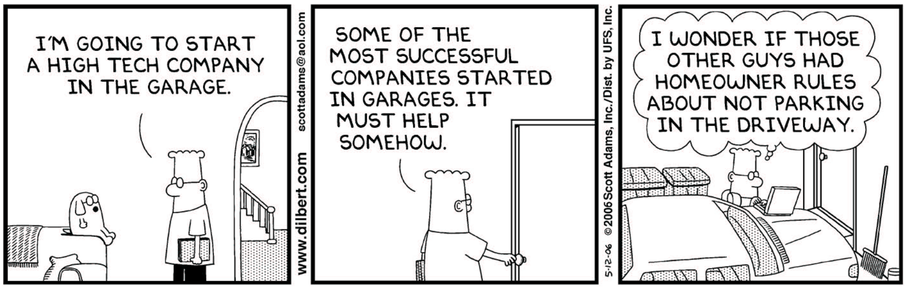
—by Robert Cravotta

▷**Stream Processors**, www.streamprocessors.com.



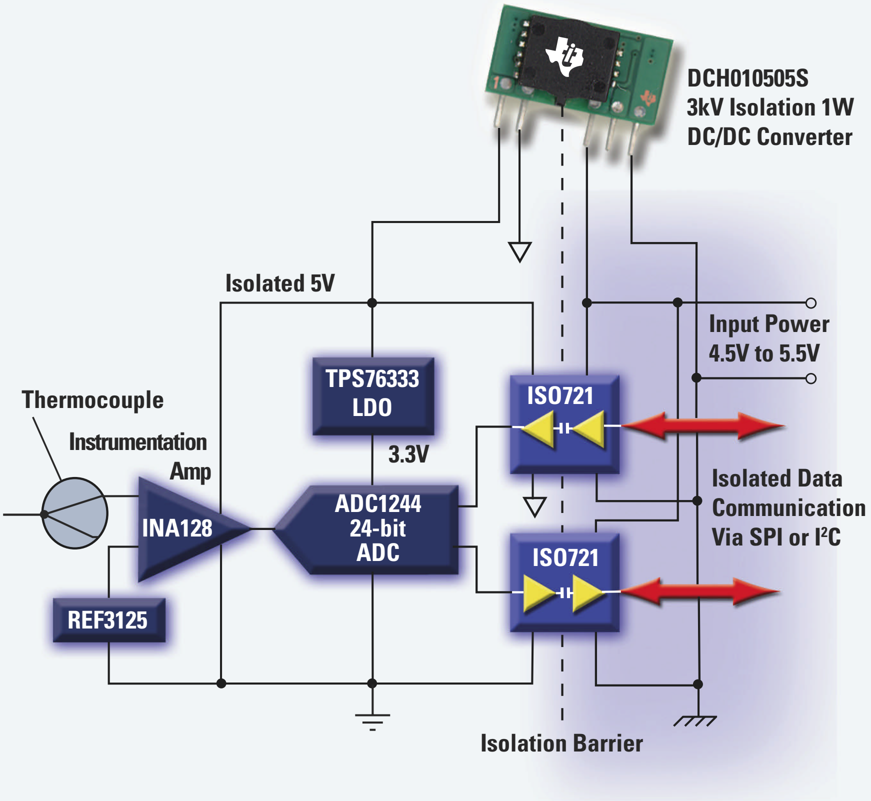
The Storm-1's multilane DPU (left) can perform as many as 80 32-bit—or, for the SP16-G160, 320 8-bit—arithmetic operations per instruction cycle. A MIPS core and the DPU make up the DSP-coprocessor subsystem (right).

DILBERT By Scott Adams



POWER MANAGEMENT

Tiny, 1W, 3kV Isolated DC/DC Converters



▶ Applications

- Data acquisition
- Industrial control and instrumentation
- Test and measurement
- Medical instrumentation
- Professional audio
- Ground loop elimination

▶ Features

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- Up to 78% efficient
- Industry standard SIP-7 package/footprint
- Single or dual output
- UL60950 certified product
- 54 million hour MTBF

The new **DCH01** DC/DC converters from Texas Instruments provide up to 1W of isolated power with 3kV isolation in an easy-to-use industry-standard SIP package. Available with single or complementary dual outputs, the DCH01 products are ideal in a variety of applications.

New DCH01 DC/DC Converters from Texas Instruments

Device	Input Voltage	Output Voltage	Output Current (mA)
DCH010505S	4.5 to 5.5	5	200
DCH010505D	4.5 to 5.5	±5	100
DCH010512S	4.5 to 5.5	12	83
DCH010512D	4.5 to 5.5	±12	42
DCH010515S	4.5 to 5.5	15	67
DCH010515D	4.5 to 5.5	±15	33

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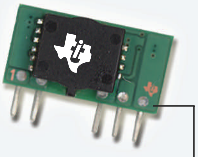

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TEXAS INSTRUMENTS

Video processor tackles diverse content

The design team that began working its video-processing magic at Faroudja (www.faroudja.com) and then moved to Sage and later Genesis Microchip (www.genesis-microchip.com) through acquisition, and, even later, to National Semiconductor (www.national.com) is now at yet another home: Marvell. (See “Video quality: a hands-on view,” *EDN*, June 7, 2001, pg 83, www.edn.com/article/CA89503 and “Video integration squashes cost, artifacts,” *EDN*, Dec 7, 2000, pg 30, www.edn.com/article/CA56179.)

The team’s first project at Marvell, the less-than-$30 (10,000) 88DE2710, which the company introduced at January’s CES (Consumer Electronics Show), has clear ties to its two National Semiconductor predecessors. Like the AVC2510, the 88DE2710 supports simultaneous standard- and high-definition-video outputs (see “Deinterlacing done high-def,” *EDN*, April 22, 2005, www.edn.com/blog/400000040/post/850000685.html). And, like the AVC5000, the 88DE2710 accepts dual high-definition video inputs (see “Two eyes, two ears, two people … two video programs?” *EDN*, Aug 20, 2005, www.edn.com/blog/400000040/post/960001296.html).

The designers have honed the video-processing blocks that lie between the inputs and the outputs through many iterations of circuit development and customer feedback. Video-processing features encompass per-pixel motion-adaptive 3-D deinterlacing, including frame-rate conversion; video-noise reduction; “block” and “mosquito” lossy-compression-artifact reduction; adaptive scaling; edge enhancement—that is, sharpening; contrast- and chroma-transient enhancement; and intelligent color remapping. (Some features apply to only one of the two input channels.) Input resolutions scale all the way from 1080p high-definition video down to 240-line material.

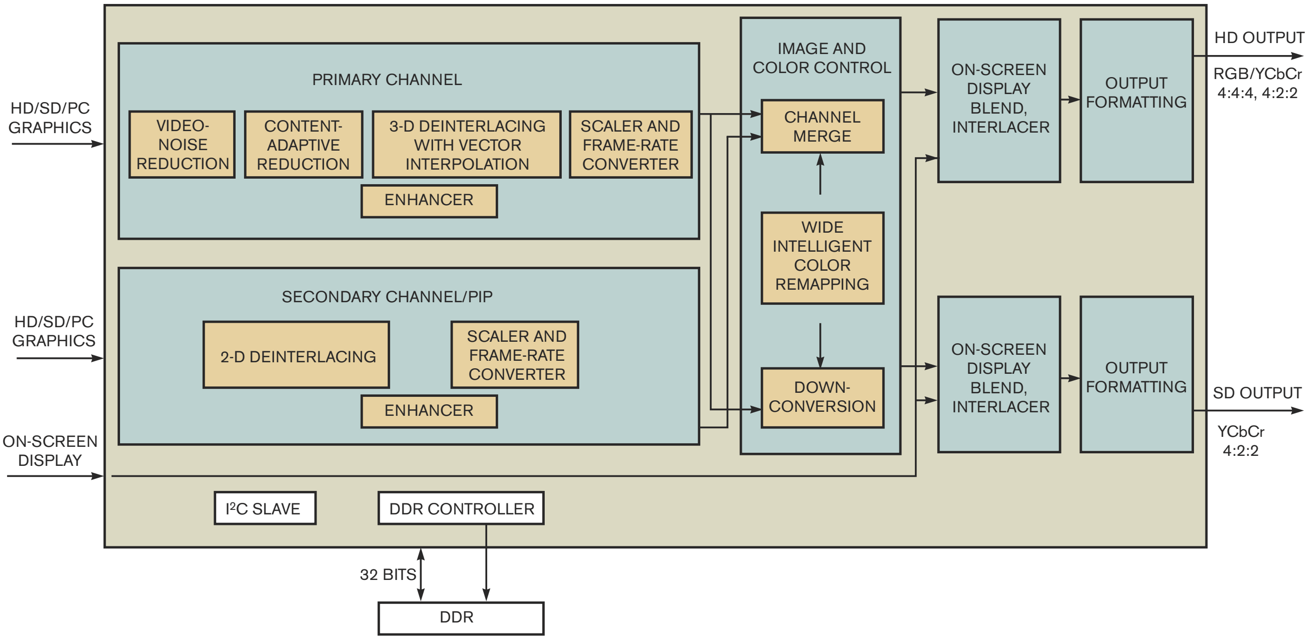
> “Regardless of this content’s native attributes, big-screen-TV owners will want it to look good on their displays.

Marvell showcased two demonstrations at CES. In the first, the 88DE2710’s algorithms visibly altered and arguably improved the low-quality, first-generation Blu-ray pressing of the movie *The Fifth Element*. The quality improvement was far more definitive in the second demo, which processed the video output of an iPod for display on a large-screen LCD.

High-definition-optical-disc competitors Blu-ray and HD DVD (high-definition digital-video disc) and a bewildering array of other high-definition-video sources, such as ATSC (Advanced Television Systems Committee), satellite, cable, and IPTV (Internet Protocol television), have been slugging it out in the marketplace. Ironically, however, the content that consumers are *most* enthusiastically embracing is low-resolution and either streamed or downloaded over the Internet from sources such as YouTube (www.youtube.com) and the iTunes Store (www.itunes.com). Regardless of this content’s native attributes, big-screen-TV owners will want it to look good on their displays, and this is the area in which the 88DE2710’s capabilities may be most compelling.

—by Brian Dipert

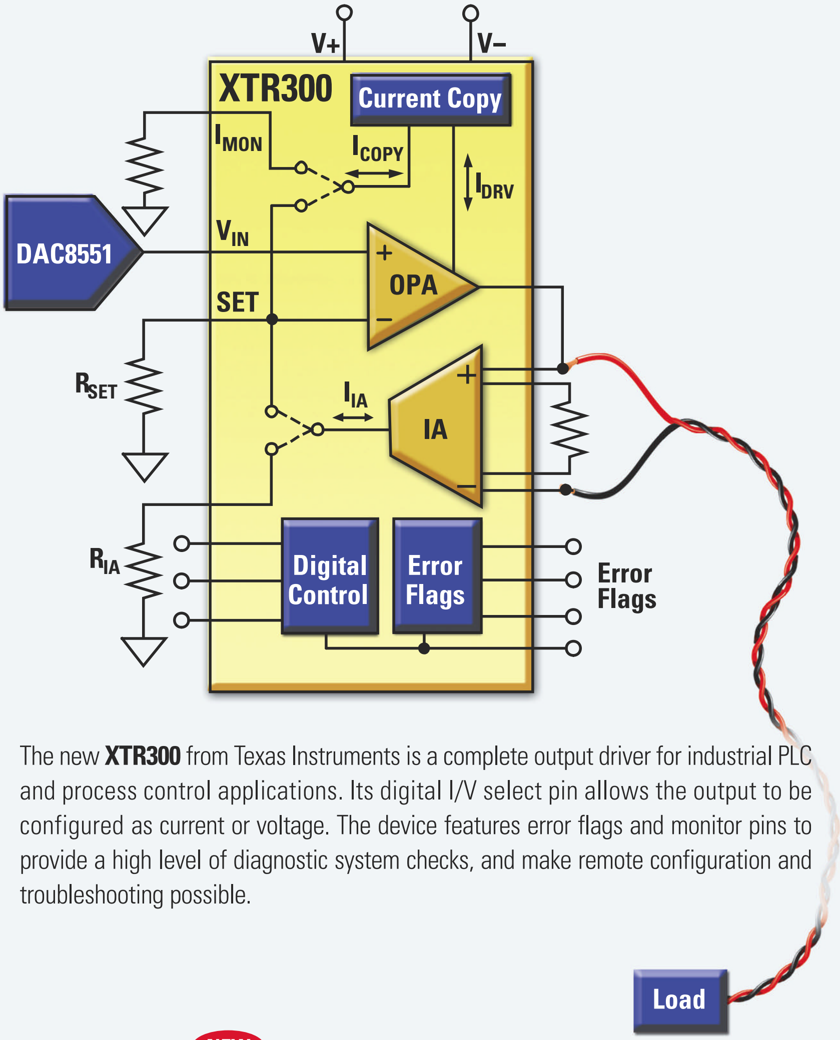
▷**Marvell**, www.marvell.com.



Marvell’s 88DE2710 focuses the bulk of its video-processing efforts on the primary high-definition input channel.

Versatile Industrial Output Driver

Voltage or Current Output



The new **XTR300** from Texas Instruments is a complete output driver for industrial PLC and process control applications. Its digital I/V select pin allows the output to be configured as current or voltage. The device features error flags and monitor pins to provide a high level of diagnostic system checks, and make remote configuration and troubleshooting possible.

Burr-Brown Products from Texas Instruments

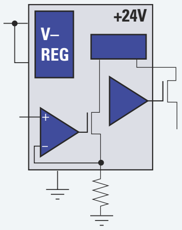
▶ Applications

- PLC output programmable driver
- Industrial cross-connectors
- Industrial high-voltage I/O
- 3-wire-sensor current or voltage output
- ±10V 2- and 4-wire voltage output

▶ Features

- User-selectable: voltage or current output
- Supply voltage: up to ±20V
- V_{OUT}: ±10V (up to ±17.5V at ±20V supply)
- I_{OUT}: ±20mA (linear up to ±24mA)
- Short- or open-circuit fault indicator pin
- No external current shunt required
- Over-current protection
- Separate driver and receiver channels
- Package: QFN-20, TSSOP-20 coming soon
- Price: $2.45 in 1k units

XTR111



NEW

The new **XTR111** is an output driver for 0-20mA or 4-20mA from a standard voltage input. It can also be connected for voltage output. It operates from 24V (up to 40V) and provides an adjustable voltage regulator output, output disable and a load error flag. Price is $1.45 in 1k.

Industrial Solutions Guide
Datasheets, Samples and
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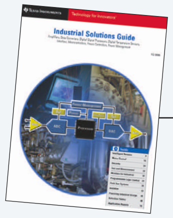

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TEXAS INSTRUMENTS

Instruments and software let you use a logic analyzer to debug serial bus

This N4850A acquisition probe, together with the N4860A stimulus probe and the 16800/900 logic analyzers running 89600A-series digital vector-signal-analysis software, enables designers of digital-RF systems to quickly verify and optimize the performance of new designs, especially wireless handsets that use the DigRF Version 3 bus between baseband and RFICs.

When you first hear about the new, 312-Mbps DigRF Version 3 bus, you might think, "What? Another new high-speed serial bus—and not even a very fast one, at that!" However, the bus has several important reasons for its existence. The bus targets use between baseband and RF chips in wireless-handheld devices—read: cell phones. With manufacturers producing nearly a billion phones annually, the cell-phone market gets whatever it wants, provided that the requirements are technically feasible. Cell phones don't need a bus with blinding speed, and chip-to-chip communication within a phone requires a bus that supports datapaths no longer than a few centimeters. But these devices do need a truly low-cost bus that uses little power when operating, offers an even lower power sleep mode, requires minimal real estate for interface circuits within baseband and RFICs, and uses as few conductors as possible to link the chips.

You may think that the potential for combining baseband and RF functions onto one chip presents a huge obstacle to the success of the DigRF bus, but DigRF's supporters disagree. Although several companies are working on one-chip phones, it is likely that approaches using separate baseband and RFICs will at least for the next few years yield lower cost phones.

DigRF makes several compromises to achieve its cost, power, and real-estate goals. Those compromises present challenges for designers of test equipment for verifying the performance of ICs that support the bus. The most important limitation is that the test instrument cannot directly verify that messages between the baseband ICs and the RFICs have arrived error free. The test instrument must reconstruct the message from information it extracts from the chip that receives the message. In this situation, Agilent's N4850A DigRF digital-serial-acquisition probe, N4860A stimulus probe for the company's 16800/900 logic-analyzer family, and 89600A-series logic-analyzer digital VSA (vector-signal-analysis) software enter the picture. With the aid of the ICs' visibility ports, the probes and software acquire and analyze internal operations and correlate microcontroller and DSP operation to DigRF traffic. By integrating these capabilities, the tools enable handset integrators to characterize the interactions between the RF and the baseband ICs to isolate defects and optimize performance.

Each probe carries a list price of $14,495. Prices for adding the VSA software to the logic analyzers start at $10,000. The software is usable with the logic analyzers but without the probes on projects involving combinations of digital and RF technology other than the DigRF Version 3 bus.

—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com/find/DigRF, www.agilent.com/find/dvsa.

PRINTER CARTRIDGE ENABLES ORGANIC ELECTRONIC R&D

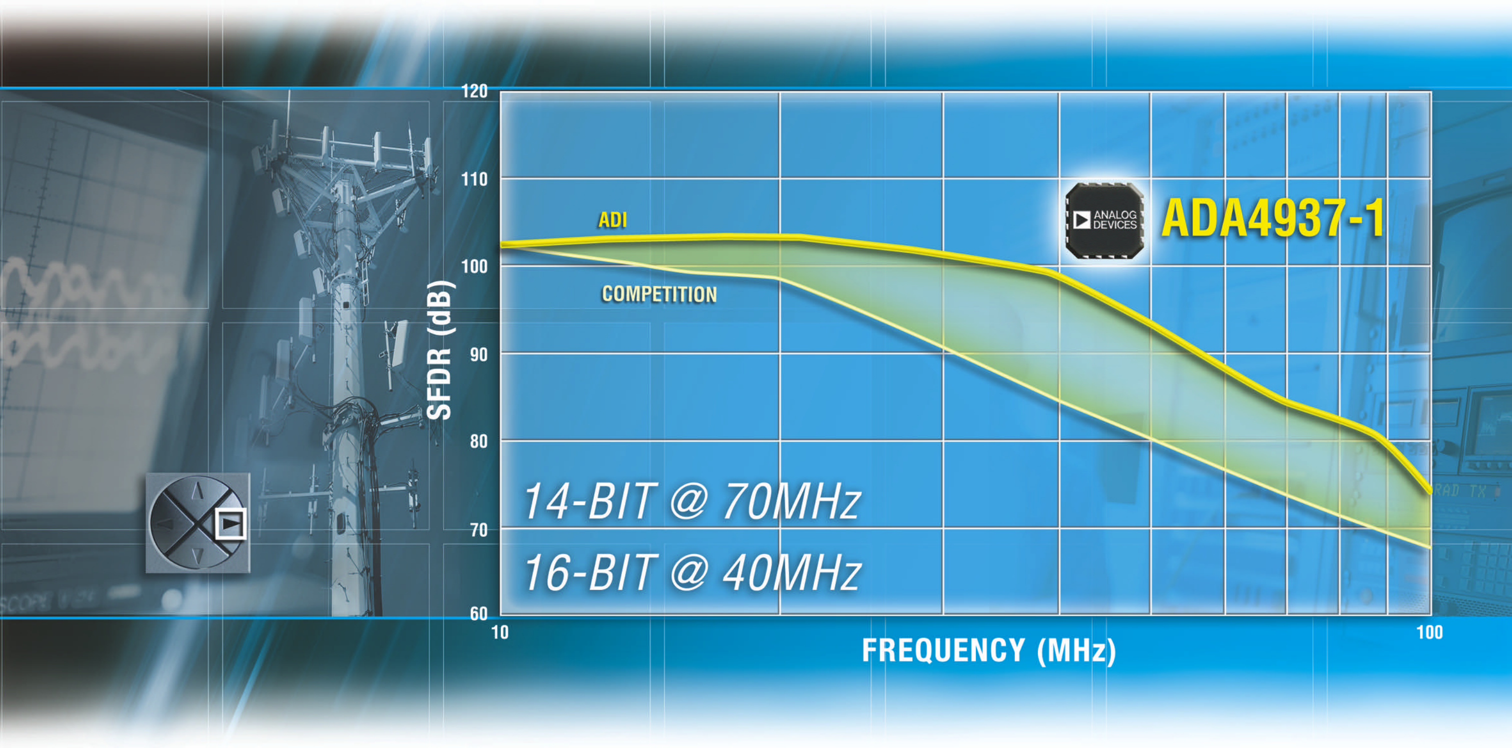
Much of the excitement about organic semiconductors and circuits centers on their polymer materials and their advantages: flexibility, low power, low cost, and low environmental impact. However, just as important to the development of this new technology is the manufacturing technology. About a year ago, Fujifilm Dimatix introduced the DMP-2800 series materials printer with a user-fillable print-head-cartridge printer that can dispense 10-pL drops. At $35,000, the printer is inexpensive enough to put the development of organic electronics within the reach of many universities and companies.

Dimatix based the print head on silicon-MEMS (microelectromechanical-system) technology. It uses a piezo effect to form an acoustic wave that forces fluid through the print-head nozzle, rather than relies on heat to "bubble" a drop from the print nozzle, as do thermal print heads. This feature provides a big advantage for organic technology, in which the fluid can't withstand the temperature rise of thermal print heads.

The original cartridge's 10-pL droplet size resulted in a 50- to 70-micron geometry, which, although thin, is still significantly larger than the desired line width of 10 microns. Dimatix has introduced a new print head and cartridge with a 1-pL drop size, resulting in 20-micron line widths, which are thin enough to create the circuits, transistors, and antennas to enable inexpensive, disposable, and flexible applications, such as displays, RFID tags, and on-chip bio labs. The 10-pL cartridge sells for $59, and the new 1-pL cartridge costs $99.—by Margery Conner

▶**Dimatix,** www.dimatix.com.

Diff amps that maximize ADC performance. With ADC drivers, analog is everywhere.



ADC	Bits	Channel Count	MSPS	Driver	
				ADA4937-1	ADA4938-1
AD9460/1	16	1	80/105/130		•
AD9446	16	1	80/100	•	•
AD9246/33	14/12	1	80/105/125		•
AD9245	14	1	20/40/65/80		•
AD9445	14	1	105/125	•	•
AD9254	14	1	150		•
AD6654	14	1	92.16	•	
AD9235/6	12	1	20/40/65/80		•
AD9230/11	12/10	1	170/210/250	•	
AD9215	10	1	65/80/105		•
AD9283	8	1	50/80/100		•
AD9480/1	8	1	250	•	
AD9640/27	14/12	2	80/105/125/150		•
AD9216	10	2	65/80/105		•
AD9288	8	2	40/80/100		•

Lowest distortion from dc to 100 MHz

The ADA4937 and ADA4938 set new differential amplifier performance standards from dc to 100 MHz. Best-in-class low noise, low distortion, high SFDR, and wide bandwidth combine to make both parts ideal for driving high speed, 12- to 16-bit ADCs. For example, now you can have true 14-bit performance at 70 MHz, and true 16-bit performance at 40 MHz. Additional features include adjustable gain and output common-mode voltage, a wide supply range, and small LFCSP packaging.

For more information on our diff amps for dc- and ac-coupled designs, please visit our website or dial 1-800-AnalogD.

ADA4937-1

- –120 dBc/–102 dBc HD2/HD3 @ 10 MHz
- –98 dBc/–100 dBc HD2/HD3 @ 40 MHz
- –84 dBc/–90 dBc HD2/HD3 @ 70 MHz
- Input voltage noise: 2.2 nV/√Hz
- –3 dB BW @ 1.6 GHz, G = 1
- 5000 V/µs slew rate
- V_S = 3.3 V to 5 V
- Price: $3.79/1k

ADA4938-1

- –112 dBc/–108 dBc HD2/HD3 @ 10 MHz
- –96 dBc/–93 dBc HD2/HD3 @ 30 MHz
- –79 dBc/–81 dBc HD2/HD3 @ 50 MHz
- Input voltage noise: 2.2 nV/√Hz
- –3 dB BW @ 1.5 GHz, G = 1
- 4700 V/µs slew rate
- V_S = 5 V to 10 V
- Price: $3.79/1k

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ANALOG DEVICES

VOICES

Summit Micro's Pat Brocket

Pat Brocket is president and chief executive officer of Summit Micro (www.summitmicro.com). Before joining Summit, Brockett was president and chief executive officer of Zarlink Semiconductor (www.zarlink.com). Previously, he spent 20 years at National Semiconductor (www.national.com) in various management roles. See additional questions and answers at www.edn.com/070315p1.

How did you get involved in technology?

A I was in fact off to college to study economics when I got my girlfriend pregnant. We decided to get married, so I had to find a decent-paying job quick! Somehow, I got accepted in the sales-trainee program at Texas Instruments and never looked back.

What was your first job in industry?

A I started taking applications phone calls and sorting through the data books to answer customer questions or find them equivalent devices. Life was a lot simpler then, with transistors, rectifiers, and diodes. I don't think I could get a sales job with Summit today!

What was your career path at National Semiconductor? What did you do to gain the respect of so many people?

A I joined National from TI in late 1979, running sales in Northern Europe. Then, I became sales manager for all of Europe, then vice president/general manager of Europe. I moved to the Santa Clara headquarters in 1989 to run worldwide sales. ... I became general manager of the analog division in 1997. I left National to become chief executive officer of Zarlink in April 2001.

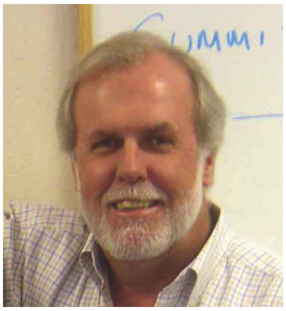
On the subject of respect, I really can't answer that question; you would have to ask the people at National. I was raised in a blue-collar family where you worked hard, told the truth, and treated people with respect.

Who was the biggest "character" you worked with at National?

A There were so many! [Analog-IC designer] Bob Widlar was brilliant and wild. Bob Swanson [general manager, analog] was tough, smart, and volatile. But, of course, the largest character there was [Chief Executive Officer] Charlie Sporck, who was a giant in many respects. I have worked with and for many tremendous people over the years.

What was at Zarlink that attracted you?

A I really wanted to be a CEO, and the opportunity came along to do that and turn around a public company.



Only a year or so after you started at Zarlink, the board of directors either forced you out or asked you to leave. The stock plunged after you left, indicating that the market did not agree with the board's decision. Can you tell us about the situation?

A I joined April Fool's Day 2001 with the goal of turning around a telecom-chip company. Revenues in 2000 were more than $500 million. By the time I had finished the June quarter, our revenue run rate was $130 million a year, and we lost $300 million for the year. Telecom went into a 'nuclear winter' and never recovered. A CEO's principal job is to enhance shareholder value. I and nobody else did during that period, so it's the board's prerogative to get rid of you if they think somebody else can do a better job.

Not long after you left Zarlink, you got involved with startup Summit Microelectronics. What made you decide to go to this small company?

A I had no interest in retiring, and the Summit board asked if I would be interested in moving the company into the consumer market. I did lots of due diligence and concluded that the technology could do well in some very-high-volume markets, so I joined. Building your own company is way more fun than sorting out someone else's. I'm the old dog surrounded by a bunch of very smart and energetic youngsters. This is a blast.

What kind of products are you working on and for what markets? What is special about the products?

A We consider ourselves world leaders in programmable power-management ICs. We're focused on the three biggest markets: communications, computing, and consumer. Our products differentiate themselves in flexibility, performance, and bill-of-materials cost. Our programmable technology puts us ahead of the competition in all three areas.

Do you still believe in Silicon Valley as a place to do business?

A Silicon Valley is the 'Rome of technology'; all roads lead here. There is a larger concentration of talent and opportunity in this valley than anywhere else in the world.

Do you see innovation in electronics happening at the same pace as it did in the early years?

A Yes, I do. When I started out, it was military and mainframes, then minis and storage. The advent of the PC began the personalization of electronics. Now, the convergence of mobile computing, telephony, and entertainment is driving even more innovative products and services. Moore's Law has ensured that every decade is more exciting than the last, and its going to continue.

What has been the biggest challenge in working in a small company?

A Actually, it's easier than working in a big company. Our entire organization is focused around doing 'killer' products for large customers quicker than the competition. Nobody is ever in doubt about what the priorities are.

—by Paul Rako

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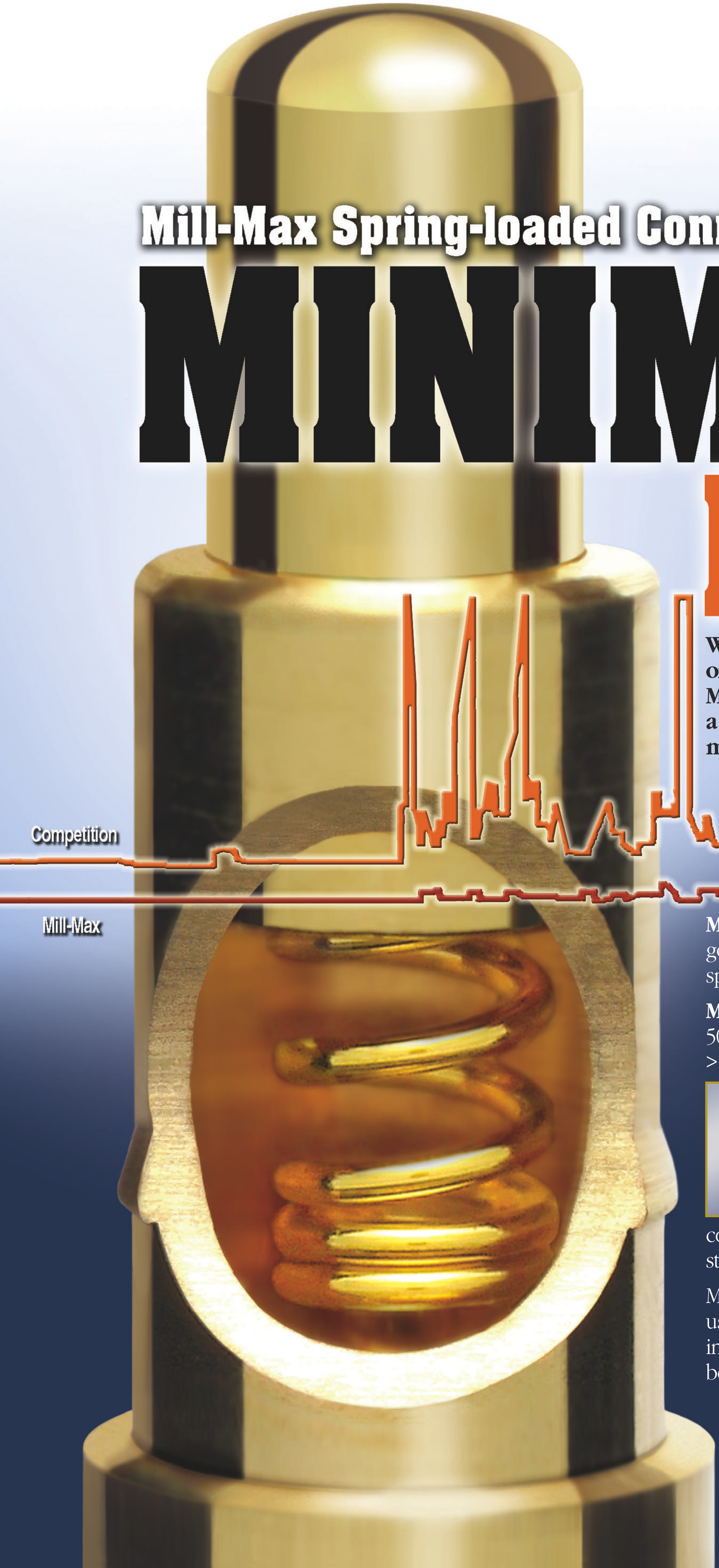

When the power is on, you don't want shock or vibration to create spurious signals. Mill-Max Spring-loaded Connectors provide a reliable electrical connection in the most rigorous environments.

Maximum Continuity: Precision-machined gold-plated components and a low-resistance spring maintain a consistent electrical path.

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Mill-Max Spring-loaded Connectors are typically used as the battery charging contacts in portable instruments, or as a rugged interconnection between circuit boards.

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BY BONNIE BAKER

IBIS and Spice timing mismatches

Growing up, I was a station-wagon kid. My parents sat in the front to see where we were going. The rest of us (six kids) took over the back, where we had a beautiful view of where we had been. Being in back wasn't bad, but input from the outside world was limited.

Similar to my parents up front, IBIS (I/O-buffer-information-specification) simulation models have a strong handle on the outside world. They model the performance of the buffer's interaction with the PCB (printed-circuit board) but omit interactions with nodes inside the chip. IBIS models simulate the system level of PCB behavior, specifically modeling the connection from the outside world to the I/O buffer. On the other hand, Spice models simulate all of the transistors inside the chip. Spice transistor-level simulations analyze the path through the output buffer but have a limited view of the PCB inductive, resistive, and capacitive parasitics.

IBIS models are high-speed and system-based. They define the elements of an IC that interact with outside, "real-world" elements. At high speeds, interactions between IC-package and PCB-trace parasitics have a strong impact on signal behavior. For instance, all models have pin and package resistive, capacitive, and inductive parasitic elements (**Figure 1**).

Why do engineers use IBIS models? Speed. IBIS models simulate 10 times faster than transistor-level models do. IBIS models offer system designers reduced analysis times and allow IC manufacturers to avoid disclosing a transistor-level netlist of the buffer, which may contain proprietary data.

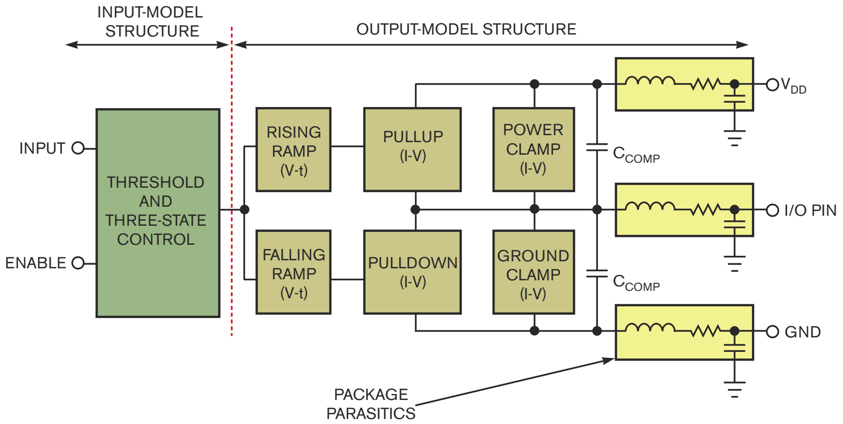

Figure 1 An IBIS model includes pin and package parasitic elements.

Concerning accuracy, current IBIS 3.2- and 4.0-model types accurately reflect CMOS-buffer impedances and switching times. Current models are ill-suited for power-delivery simulations, although improvements are coming. Otherwise, the model is as accurate as its source. If you generate an IBIS model from benchtesting the silicon, it can't simulate maximum and minimum statistical borders. The Spice-generated model is most accurate when IC designers carefully revisit their transistor models after collecting silicon bench data.

Simulating an IBIS model alongside its transistor-level Spice counterpart creates a mismatch between the IBIS- and Spice-simulation waveforms. A difference may exist between the initial delay of the waveforms—the time the output begins to switch minus the initial start time, t_0, of the simulation output curves. This scenario can occur even when IBIS and Spice models use the same excitation signals and load. This concept may be disconcerting at first, but closer inspection shows a shift in time between the two sets of waveforms. Why? Because the IBIS model is the "front-seat driver." As the back-seat kid, the Spice model includes the entire delay through the output buffer, and the IBIS model represents only the buffer's external behavior. The difference in initial delays between the Spice and IBIS models doesn't matter, because the model user always "normalizes" delays to a reference condition.

The correlation between IBIS and Spice models may not be 100%, but speed advantages make IBIS models useful tools for system analysis.**EDN**

REFERENCES

Visit www.edn.com/070315bb for this column's associated references.

Bonnie Baker is a senior applications engineer at Texas Instruments. You can reach her at bonnie@ti.com.

BY MARVIN COLLINS

Serendipity revisited

DANIEL VASCONCELLOS

Years ago, I was the studio supervisor for an AM-radio station, where part of my responsibility was to maintain the technical equipment in good operating condition. I can no longer remember the problem I encountered on this particular day. However, I do recall that the solution to the problem required a particular capacitor. I remember going to the parts-storage cabinet at the radio-station studio and putting a couple of capacitors in my pocket that I believed could fix the problem. They did, and I drove home after quitting time.

Upon arrival at home, I parked my car outside and entered the house through the front door. My wife greeted me and immediately reported that our garage-door opener would not open the garage door. This problem might seem small, but those of you who have been married for a while know that for a wife who brings home groceries through the garage to the kitchen, the garage door better open when commanded. A husband's life will be a lot better if he immediately takes care of this problem.

My first suspicion was that the garage-door transmitter in my wife's car needed new batteries. However, my voltmeter indicated proper battery voltage. Next, I tried to open the garage door with the transmitter in *my* car. It did not open.

My suspicion now turned to the receiver for the garage-door opener. I should mention that my garage-door opener is a Heathkit product that I put together myself. The advantage of building from a kit is that I have good documentation, including a schematic of the receiver. After looking at the receiver schematic and making a few measurements, I started to think the problem was a failed coupling capacitor. I soon found the capacitor to be open.

The capacitor had both leads coming out of the same end and soldered onto a PCB (printed-circuit board). As I looked at the failed capacitor, I thought it looked familiar. Suddenly, I remembered the capacitors I had been working with earlier in the day at the radio station. I also remembered that I still had an extra one in my pocket. Now comes the best part: It was the *exact* replacement for the failed capacitor in my garage-door-opener receiver—same brand, value, shape, and color. Installing the capacitor from my pocket fixed the problem.

This serendipitous repair occurred about 40 years ago. Heathkit's product line is long gone, but my Heathkit garage-door opener is still opening and closing my garage door after all these years. That night, I was my wife's hero for fixing the garage door. Serendipity saved the evening. **EDN**

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- Marvin was inspired to share his capacitor tale after reading Billy Sevel's tale, "Serendipity saves the day," at www.edn.com/article/CA6382669.
- Go to www.edn.com/070315tales to post a comment on this tale.

Marvin Collins is now a retired radio-station engineer after having been in the business for more than 50 years, the last 20 of which he served as chief engineer of KFI-KOST in Los Angeles. Like Marvin, you can share your Tales from the Cube and receive $200. Contact Maury Wright at mgwright@edn.com.

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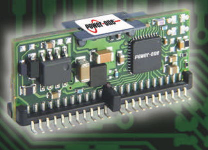

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DPA & IBA Bricks

Applications	Solutions
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	Pin-strapable Z-1000 POLs provide digital power management capabilities without software or external controllers.
Analog Point-Of-Load Conversion	Y-Series POL converters are available in industry-standard and high-performance Power-One footprints.
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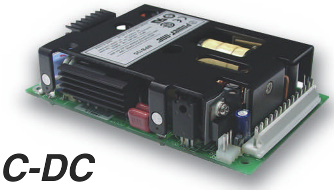
System-Level DPA and IBA	AC-DC front ends in hot-swap power shelf and chassis-mount configurations.
Centralized Architectures	Single and multiple output models include flexible modular solutions.
Industrial and Transportation	Rugged cassette style and DIN-Rail mount AC-DC and DC-DC products.
CompactPCI	AC-DC and DC-DC in 3U and 6U form factors.

AC-DC Front Ends



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PRYING EYES BY ROBERT CRAVOTTA • TECHNICAL EDITOR

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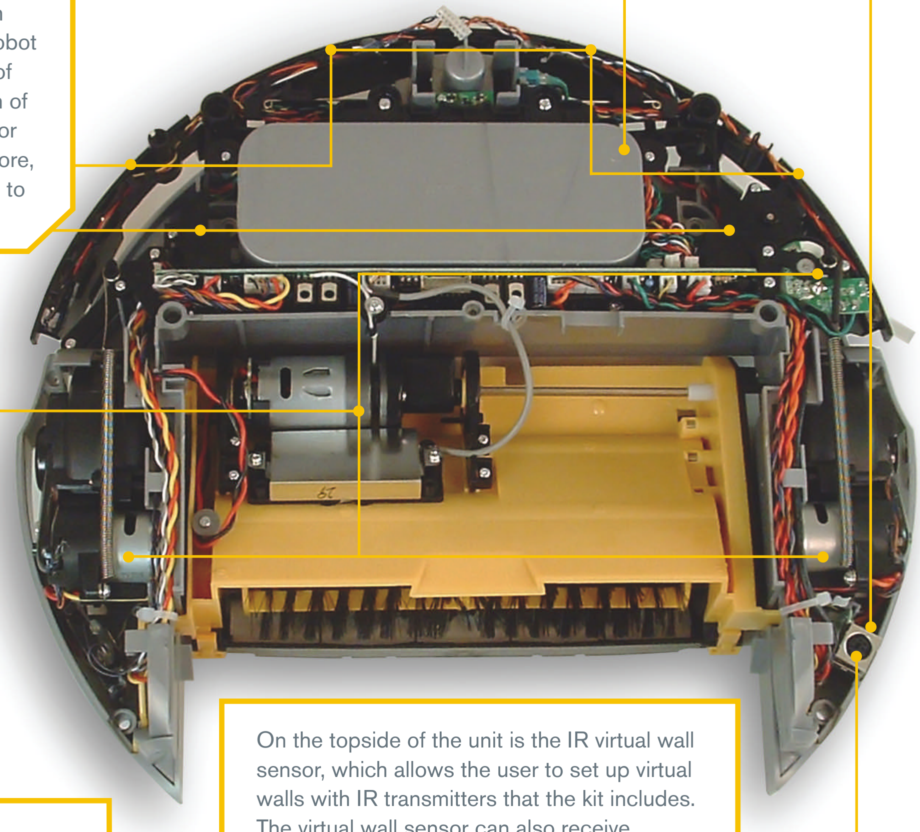
Go to www.edn.com/070315pry for additional photos of the Roomba.

Rummage through a Roomba

The Roomba from iRobot (www.irobot.com) is an autonomous vacuuming robot for use in consumers' homes. The unit is a circular robot that measures less than 14 in. in diameter and less than 3 in. in height. The Roomba can clean hardwood floors and carpets, get dirt from under furniture, avoid stairs, and return to its docking station to recharge its battery. To date, iRobot has sold more than 2 million of the robots worldwide. The Roomba relies on iRobot's Aware Robot Intelligence System, which manages the robot's sensors and can adjust the control systems as many as 67 times per second.



The 14.4V nickel-metal-hydride-battery pack is the largest and heaviest single component in the robot. The user can charge the battery directly through the battery-charger socket or through the contact points with the home base station.

Four IR cliff sensors reside around the front bottom of the unit. If the robot cannot detect a bounce back of the IR signal, it assumes it is on a cliff or stair edge and changes its behavior to avoid falling off. Inside the unit are two IR sensors working with two paddles, each containing a window, to detect when the robot has collided with something. The position of the sensors and the mechanical orientation of the robot frame does not detect collisions or cliffs if the unit is moving backward. Therefore, the proper behavior to moving backward is to rotate the robot and then move it forward.

The Roomba contains four motors. A separate motor drives each of the large side wheels. No motor drives the front caster wheel, as it provides only stability and not any locomotive force to the robot. A smaller motor drives the two counter-rotating brushes to capture large debris. The smallest motor spins the edge-cleaning side brush, which pushes dirt on wall and furniture edges into the cleaning path of the robot.

IRobot offers a Command Module (not shown) that uses an 8-bit, 20-MHz (Atmel ATMega 168) microcontroller to expand how third-party developers can interact with the unit's onboard microcontroller, motors, lights, sounds, and sensor readings with software written in C or C++.

On the topside of the unit is the IR virtual wall sensor, which allows the user to set up virtual walls with IR transmitters that the kit includes. The virtual wall sensor can also receive signals from the home base station and the handheld remote-control unit (not shown). On the side of the unit is an IR wall sensor, so that the robot can adjust its behavior to clean along walls and furniture. An accessible serial-port interface allows home developers to program the unit for other uses.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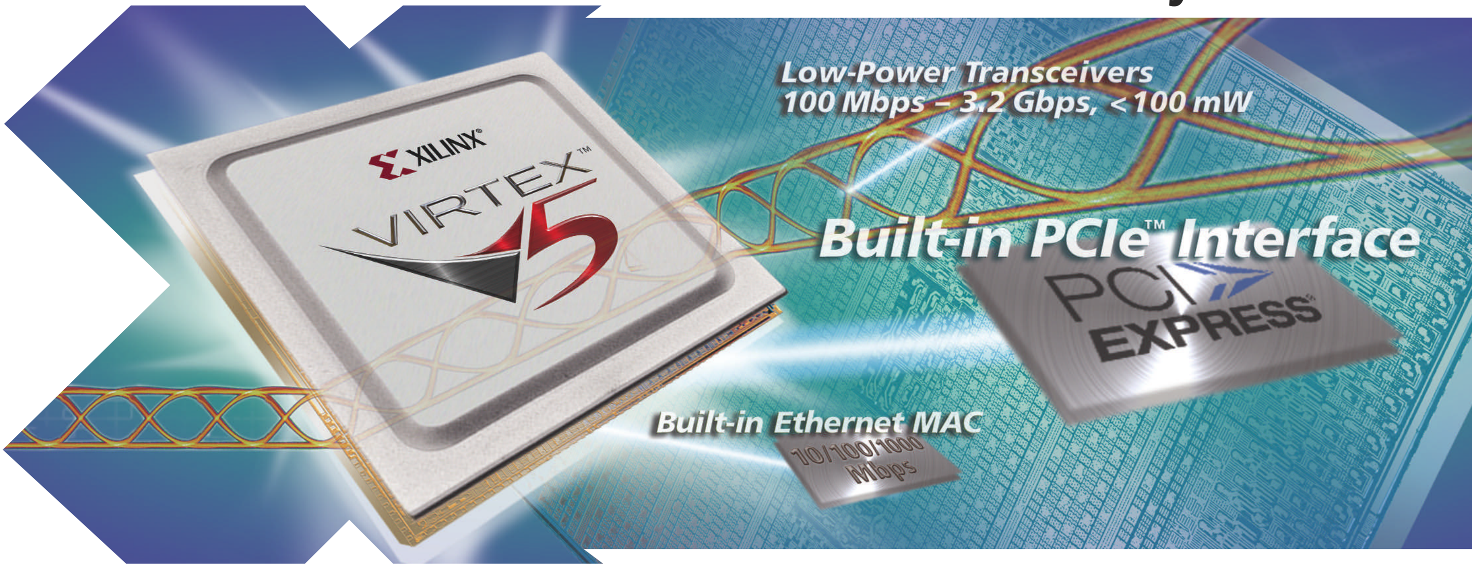

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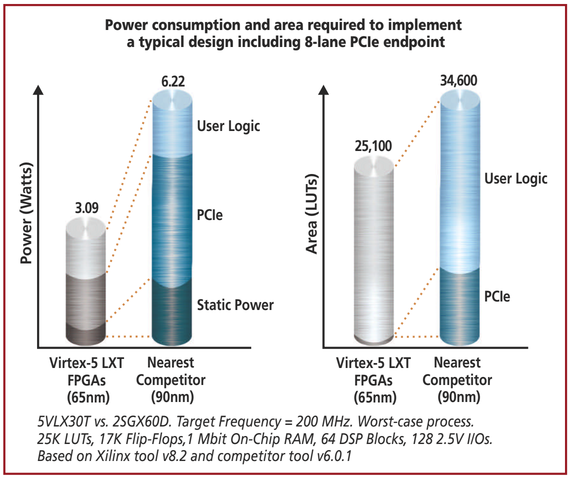

5VLX30T vs. 2SGX60D. Target Frequency = 200 MHz. Worst-case process. 25K LUTs, 17K Flip-Flops,1 Mbit On-Chip RAM, 64 DSP Blocks, 128 2.5V I/Os. Based on Xilinx tool v8.2 and competitor tool v6.0.1

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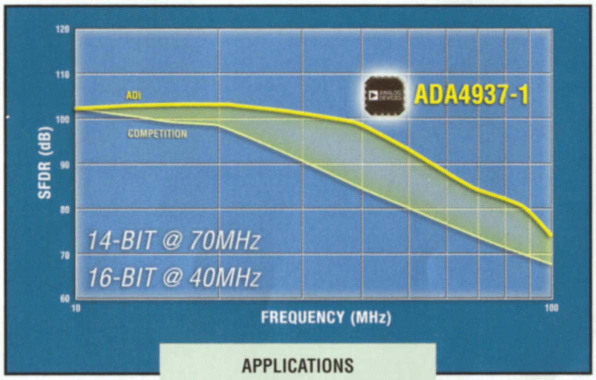
ADC Drivers Set New Distortion Performance Standards: 14-Bits @ 70 MHz, 16-Bits @ 40 MHz

Special Offer
3rd Edition,
A Designer's Guide to Instrumentation Amplifiers—
Hot Off the Press

The ADA4937-1 and ADA4938-1 set new performance standards in noise and distortion for differential ADC drivers. The devices enable design engineers to easily get the most out of their high performance ADCs since amplifier distortion will not limit system performance. The adjustable level of the output common mode allows the ADA4937-1 and ADA4938-1 to match the input of the ADC.

The internal common-mode feedback loop also provides exceptional output balance as well as suppression of even-order harmonic distortion. Full differential and single-ended to differential gain configurations are easily realized. A simple external feedback network of four resistors determines the amplifier's closed-loop gain.

The ADA4937-1 works on a 3 V to 5 V supply range. It is specified to operate over the temperature range of –40°C to +105°C. The ADA4938-1 works on a 5 V to 10 V supply range and is specified to operate over the industrial temperature range of –40°C to +85°C.



APPLICATIONS

- ADC drivers
- Single-ended to differential converters
- IF and baseband gain blocks
- Differential buffers
- Line drivers

ADA4937-1	$3.79
ADA4938-1	$3.79

ADA4937-1

- –120 dBc/–102 dBc HD2/HD3 @ 10 MHz
- –98 dBc/–100 dBc HD2/HD3 @ 40 MHz
- –84 dBc/–90 dBc HD2/HD3 @ 70 MHz
- –3 dB BW @ 1.6 GHz, G = 1
- Slew rate: 5000 V/μs
- V_S = 3.3 V to 5 V

ADA4938-1

- –112 dBc/–108 dBc HD2/HD3 @ 10 MHz
- –96 dBc/–93 dBc HD2/HD3 @ 30 MHz
- –79 dBc/–81 dBc HD2/HD3 @ 50 MHz
- –3 dB BW @ 1.5 GHz, G = 1
- Slew rate 4700 V/μs
- V_S = 5 V to 10 V

ADA4937-1 and ADA4938-1

- Input voltage noise: 2.2 nV/√Hz
- dB gain flatness to 125 MHz
- Fast settling to 0.01% in 8 ns
- 3 mm × 3 mm LFCSP

Driver Amplifiers for Selected High Speed, High Performance A/D Converters

ADC	Bits	Channel Count	MSPS	Driver	
				ADA4937-1	ADA4938-1
AD9460/AD9461	16	1	80/105/130		•
AD9446	16	1	80/100	•	•
AD9246/AD9233	14/12	1	80/105/125		•
AD9245	14	1	20/40/65/80		•
AD9445	14	1	105/125	•	•
AD9254	14	1	150		•
AD6654	14	1	92.16	•	
AD9235/AD9236	12	1	20/40/65/80		•
AD9230/AD9211	12/10	1	170/210/250	•	
AD9215	10	1	65/80/105		•
AD9283	8	1	50/80/100		•
AD9480/AD9481	8	1	250	•	
AD9640/AD9627	14/12	2	80/105/125/150		•
AD9216	10	2	65/80/105		•
AD9288	8	2	40/80/100		•

"Design Considerations in Specifying Data Converters for High Speed Applications" at *www.analog.com/onlineseminars*.

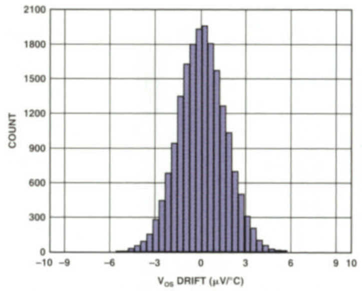
Optimize your high speed design with ADI's free online virtual evaluation tool. Go to *www.analog.com/ADIsimADC*.

High Voltage, Bidirectional Current Sense Amplifier with Guaranteed Accuracy Over the Operating Temperature Range

The AD8210 single-supply, bidirectional current shunt monitor amplifies small input differential voltages while rejecting large common-mode voltages from −2 V to +65 V. It is ideal for battery management, precision motor control, power distribution, and solenoid control applications.

The AD8210 offers very high precision and guaranteed min-max specifications for key parameters such as CMRR, offset drift, and gain drift from −40°C to +125°C. The output amplifier can be offset to any point within the 5 V supply range by connecting the two user-accessible, precision offset pins to the supply of the AD8210, GND, an external reference, or the supply of other components, such as the ADC.

AD8210
LOW GUARANTEED OFFSET DRIFT



APPLICATIONS

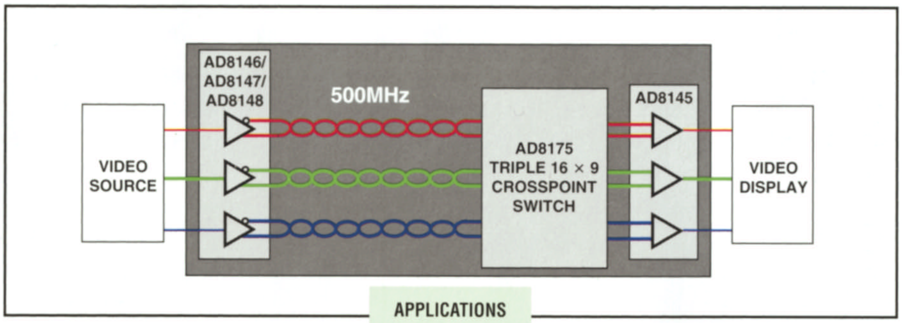
- Battery charge/discharge
- H-bridge motor control
- 3-phase motor control
- Solenoid control
- Power distribution systems

Part Number	Common-Mode Range (V)	Bandwidth (kHz Typ)	DC CMRR (dB)	Gain	Supply Voltage (V)	Offset (mV)	VosiTC (µV/°C) Max	Gain Tempco (ppm /°C)	Temperature Range (°C)	Price
ADI's high performance current sense amplifiers support a wide range of industrial and automotive applications										
AD8206	−2 to +65	100	76	20	5	±2	15	30	−40 to +125	1.35
AD8210	−2 to +65	450	120	20	5	±1	8	20	−40 to +125	1.79
AD8212	7 to 65*	450	90	Adj	7 to 65*	±2	15	30	−40 to +125	0.92
AD8214	5 to 65	N/A	80	Adj	5 to 65	±1	15	30	−40 to +125	0.75

*The AD8212 supply/common-mode range can be extended by using an external PNP transistor. The V_{BE} breakdown of this transistor becomes effective supply/common-mode voltage range.

Achieve a True UXGA Resolution via RGB Video Distribution Solution

Designers of video distribution and KVM solutions who need to achieve true end-to-end UXGA system performance, face increasing bandwidth requirements to ensure signal integrity. The AD8175 crosspoint switch and AD8145, AD8146, AD8147, and AD8148 triple differential amplifiers offer >500 MHz bandwidth—a 40% increase over competitive components. Higher bandwidth through the entire signal chain equates to better image quality for end customers.



APPLICATIONS

- KVM
- Video distribution

Part Number	BW (MHz)	Gain	Description	Price
AD8145	550*	1 or 2	Triple differential-to-single amplifier with 2 comparators	2.89
AD8146	700*	2	Triple differential amp with uncommitted common mode	2.89
AD8147	700*	2	Triple differential amp with sync on common mode	2.99
AD8148	540*	4	Triple differential amp with sync on common mode	3.09
AD8175	500	2	Differential in/out, triple 16:9 crosspoint switch	95.00
AD8176	500	4	Differential in/out, triple 16:9 crosspoint switch	95.00

*—2 V p-p, 3 dB bandwidth

1:2 Single-Ended, Low Cost, Active CATV RF Splitter Simplifies Design and Improves Performance

The ADA4303-2 is a 75 Ω 2-output active splitter for use in applications where a lossless signal split is required. It is ideal as a replacement for those traditional solutions that require discrete passive splitter modules with separate fixed-gain, low noise amplifiers.

The ADA4303-2 is a low cost alternative that simplifies designs and improves system performance by integrating a signal splitter and a gain block into a single IC. The device operates in the extended industrial temperature range of −40°C to +85°C and is available in a 12-lead LFCSP.

- Excellent frequency response:
  - 1.7 GHz, −3 dB bandwidth
  - 1 dB flatness to 1.2 GHz
- Low noise figure: 4.4 dB
- Low distortion:
  - Composite second order (CSO): −62 dBc
  - Composite triple beat (CTB): −72 dBc
  - 1 dB compression point of 8.5 dBm
- 3 dB of gain per output channel
- 75 Ω inputs and outputs
- 12-lead, 3 mm × 3 mm LFCSP

APPLICATIONS

- Multituner digital set-top boxes
- Cable splitter modules
- Multituner/digital cable ready (DCR) TVs
- Home gateways

ADA4303-2

$0.63
at 100k unit

Micropower, Low Voltage, Sub Band Gap, Precision Voltage Reference in Tiny TSOT

Low voltage in a small footprint is a key requirement to support long battery life in portable, battery-operated instrumentation. The ADR130 voltage reference is capable of delivering a continuous output voltage at either .5 V or 1.0 V with a supply current of 150 μA max at the lowest frequency noise of 3 μV p-p (0.1 Hz to 10 Hz). It features 0.35% initial accuracy and 25 ppm/°C of temperature drift, and only requires 80 μA for typical operation.

The ADR130 design includes a patented temperature drift curvature correction technique that minimizes the nonlinearities in the output voltage vs. temperature characteristics. This technique provides a stable output voltage optimized for high speed 3 V ADCs including the AD9228, AD9246, and the AD9248 that require either a .5 V or 1.0 V reference input. The ADR130 is specified over the industrial temperature range of –40°C to +125°C.

Part Number	V_{OUT} (V)	Initial Accuracy %	Tempco (ppm/°C)	Supply Voltage (V)	Supply Current (μA)	Output Current (mA)	Output Noise (μV p-p)	Package	Price
ADI's ADR1xx family of precision, low voltage references									
ADR121	2.5	.12	9	2.8 to 18	95	+5/–2	10	TSOT	.77
ADR125	5	.12	9	5.3 to 18	95	+5/–2	20	TSOT	.77
ADR127	1.25	.12	9	2.7 to 18	95	+5/–2	5	TSOT	.77
ADR130	.5, 1.0	.35	25	2 to 18	150	+4/–2	3	TSOT	.97

Precision, Low Cost, Micropower CMOS Op Amps Ideal for Battery-Powered Applications

With its low power consumption, low input bias current, and rail-to-rail input/output, the AD850x family is ideally suited for a variety of battery-powered portable applications. The device's low offset voltage supports systems with high gain while minimizing excessively large output and offset errors. The AD850x offers high accuracy without the need for system calibration. Rail-to-rail I/O helps maximize dynamic range and signal-to-noise ratio in systems that operate at very low voltages. The AD850x family is fully specified for –40°C to +85°C and is operational over –40°C to +125°C. The AD8502 is available in an 8-lead SOT-23; the AD8504 is available in a 14-lead TSSOP.

AD850x specifications:

- Low power: 1 μA per channel
- Low offset voltage: 3 mV max
- Low input bias current: 10 pA max
- CMRR: 76 dB
- PSRR: 105 dB

Part Number	Number of Amps	Min	Max	BW @ A_{CL} Min (kHz)	V_{OS} Max (mV)	Noise (nV/√Hz)	Supply Current per Amp (μA Typ)	Package*	Price @ 100k
Low power, low voltage, low cost op amps optimized for portable applications									
AD8541	1	2.7	6	1000	6	40	38	SOT-23	0.20
AD8542	2	2.7	6	1000	6	40	38	SOIC	0.30
AD8544	4	2.7	6	1000	6	40	38	SOIC	0.45
AD8538	1	2.7	6	600	0.013	50	150	SOT-23	0.67
AD8613	1	1.8	6	400	2	25	38	SOT-23	0.29
AD8617	2	1.8	6	400	2	25	38	SOIC	0.45
AD8619	4	1.8	6	400	2	25	38	SOIC	0.71
AD8607	2	1.8	6	400	0.05	25	40	SOIC	0.66
AD8609	4	1.8	6	400	0.05	25	40	SOIC	1.28
AD8500	1	1.8	6	7	1	160	1	SC70	0.51
AD8502	2	1.8	6	7	1	160	1	SOT-23	0.41
AD8504	4	1.8	6	7	3	190	1	TSSOP	0.58

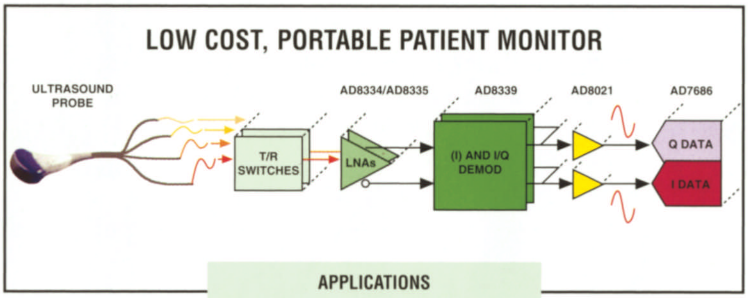
*Other packages may be available. Contact ADI.

Reduce Component Count and Power Consumption with Quad I/Q Demodulator and Phase Shifter for CW Doppler

The AD8339 low power, quad I/Q demodulator is optimized for continuous wave (CW) doppler analog beam forming in low power applications such as portable medical ultrasound. It provides coherent summing and phase alignment of multiple input channels in 22.5° increments, selected independently for each of the four channels. In the past, beam formers have been implemented using delay lines, crosspoint switches, and amplifiers—solutions that have proven space consuming, power hungry, and costly. With the single chip AD8339 solution, available in a 6 mm × 6 mm, 40-lead LFCSP, designers can reduce board space, power, and cost over such traditional solutions.

An SPI®-compatible serial interface is provided for ease of programming the phase of each channel. It also allows for power-down of each individual channel and the complete chip. The AD8339 is specified from –40°C to +85°C.

- Power consumption: 73 mW/channel
- Dynamic range: 158 dB/Hz/channel
- Quadrature phase error: ±1°
- I/Q amplitude imbalance: ±0.25 dB
- Frequency range:
  - 4 LO: 100 kHz to 100 MHz
  - RF: dc to 25 MHz
- Supply: ±5 V



AD8339

APPLICATIONS

- Medical imaging (CW ultrasound beam forming)
- Phased array systems
- Radar
- Adaptive antennas
- Communication receivers

$11.95

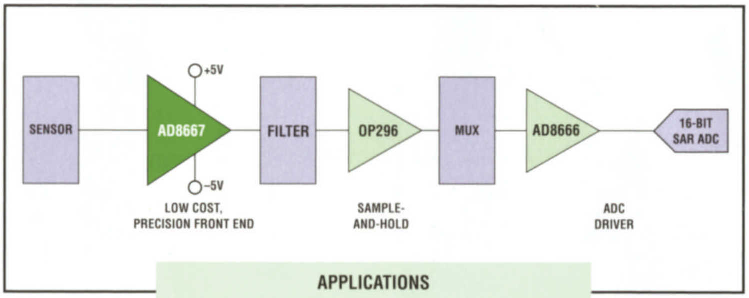
Online seminar available on demand: "Enabling the Next Generation of Medical Instrumentation" at *www.analog.com/onlineseminars*.

Rail-to-Rail Op Amp that Meets Your Low Power, High Voltage Design Requirements

*i*CMOS™ INDUSTRIAL

The AD8667 dual, rail-to-rail output op amp offers industry-leading precision, power, and noise performance, making it ideal for medical and instrumentation applications. The device is manufactured on ADI's *i*CMOS® manufacturing process—a technology that combines high voltage silicon with submicron CMOS and complementary bipolar technologies, enabling this product to deliver guaranteed tested precision for both single-supply (5 V to 16 V) and dual-supply operation (±2.5 V to ±8 V) at a great price. The AD8667 is available in an 8-lead SOIC and MSOP.

- Low power: 250 μA
- Voltage offset: 100 μV maximum
- Bias current : 1 pA
- Voltage noise: 23 nV/√Hz
- Gain bandwidth: 550 kHz



AD8667

APPLICATIONS

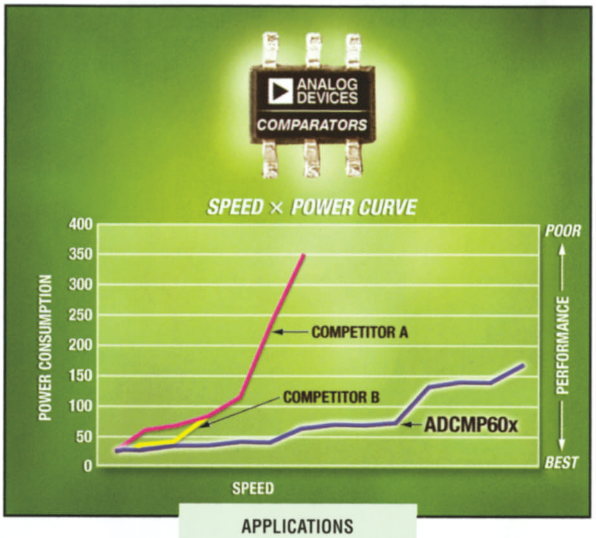
- Medical equipment
- Physiological measurement
- Buffer/level shifting
- Portable operated systems
- High density power budget systems
- Multipole filters
- Photodiode amplification
- ADC driver

$0.73
@ 100k unit

Versatile, 2.5 V to 5.5 V, Single-Supply, Rail-to-Rail Comparators Feature Industry's First LVDS Output

The ADCMP60x family of rail-to-rail comparators is designed for applications that require high speed, low power, rail-to-rail swing, and high precision. All prevailing digital output stages are supported including LVDS, CML, and TTL/CMOS. The ADCMP60x family offers propagation delays ranging from 1 ns to 35 ns, with as little as 2.0 ps rms random jitter. Rail-to-rail performance is fully specified from 2.5 V to 5.5 V. These comparators are ideal for level translation; simply select the comparator that has sufficient input voltage range and the correct output type.

ADCMP60x comparators work well in applications with ADI's family of DDS products—including the AD9911—to generate programmable high speed, low jitter clocks. They also complement ADI's high speed log amps, such as the AD8318, for amplifying low level RF burst pulses.



APPLICATIONS

- Medical instrumentation
- Test and measurement
- Telecommunications equipment
- Wireless communications

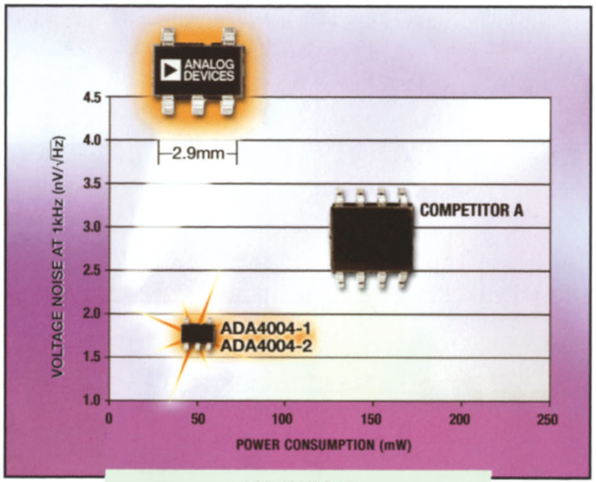
Part Number	Prop Delay (ns)	Total Power	Supply (V)	Input Range	Package	Output Type	Price
ADCMP600/ADCMP601/ ADCMP602/ADCMP603	3	6	2.5 to 5.5	-0.5 to $V_{CC} + 0.2$ V	SC70, SOT-23, MSOP, LFCSP	TTL/CMOS	1.70
ADCMP604/ADCMP605	1.5	42	2.5 to 5.5	-0.5 to $V_{CC} + 0.2$ V	SC70, LFCSP	LVDS	2.15
ADCMP606/ADCMP607	1	62	2.5 to 5.5	-0.5 to $V_{CC} + 0.2$ V	SC70, LFCSP	CML	2.35
ADCMP608/ADCMP609	30	1	2.5 to 5.5	-0.5 to $V_{CC} + 0.2$ V	SC70, MSOP	TTL/CMOS	0.58

Low Cost, Low Noise, 36 V, Precision Op Amps in Tiny SOT-23

iPOLAR INDUSTRIAL

The ADA4004-1 and ADA4004-2 offer industry-leading 1.8 nV/√Hz noise performance at just 1.7 mA/amp of supply current. This combination allows the best dynamic range over the extended industrial temperature range without incurring additional cooling or power penalties (for example, fans or heat sinks). The SOT-23 package saves board space, reduces cost, and improves layout flexibility. The ADA4004-1 (single) and ADA4004-2 (dual) are fully specified to operate from ±4 V to ±18 V.

- Low voltage noise: 1.8 nV/√Hz
- Supply current: 1.7 mA
- Offset voltage: 140 μV max
- Extended temperature range: –40°C to +125°C
- Single available in 5-lead SOT and 8-lead SOIC
- Dual available in 8-lead MSOP



APPLICATIONS

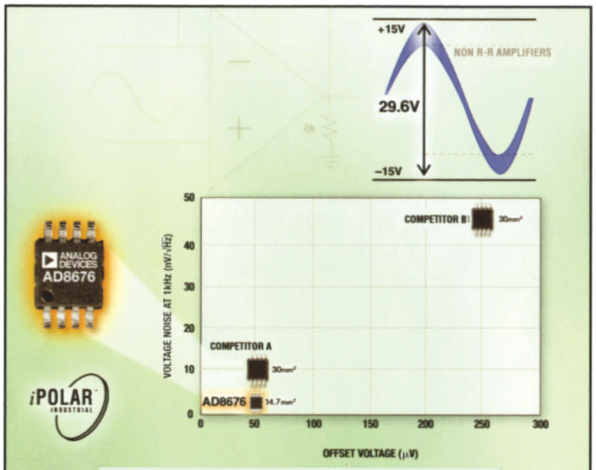
- PLL loop filters and filter blocks
- Control loops
- Reference buffering
- Thermocouple sensors and controls
- Load monitors

ADA4004-1	$0.90
ADA4004-2	$1.59

36 V, 2.8 nV/√Hz, Rail-to-Rail Output Op Amp Offers Accuracy and Resolution in Industrial and Instrumentation Applications

*i*POLAR™ INDUSTRIAL

The AD8676 high precision dual amplifier is ideal for applications that require low noise, dc precision, and rail-to-rail output swing to maximize SNR and dynamic range. With typical offset voltage of only 10 μV, offset drift of 0.2 μV/°C, and noise of only 0.10 μV p-p (0.1 Hz to 10 Hz), the AD8676 provides exceptional dc and ac accuracy and resolution.



APPLICATIONS

Precision instrumentation	Strain gage amplifiers
PLL filters	Medical instrumentation
Laser diode control loops	Thermocoupler amplifiers

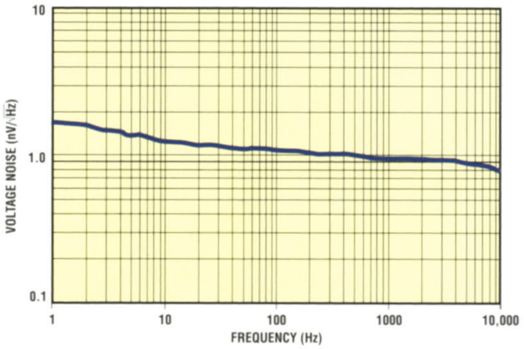
The AD8676 is specified to operate from ±5 V to ±15 V and from –40°C to +125°C. It is available in an 8-lead MSOP and narrow SOIC, Pb-free packages.

- Low noise: 2.8 nV/√Hz
- Low offset voltage: 50 μV max
- Bandwidth: 10 MHz
- Offset voltage drift: 0.6 μV/°C max
- High CMRR: 130 dB
- High PSSR: 120 dB for ±5 V to ±15 V
- Input bias current: 2 nA max
- AD8676 A-grade (100 μV): $1.64
- AD8676 B-grade (50 μV): $2.11

Lowest Noise, 36 V, Dual Op Amp

*i*POLAR™ INDUSTRIAL

Reducing preamp noise in design is crucial to the overall system noise budget. The AD8599 offers low noise of 1 nV/√Hz at 1 kHz and –100 dB low harmonic distortion, ideal for dc to high fidelity audio, medical, and precision instrumentation accuracy requirements. Using ADI's unique *i*Polar™ process technology, the AD8599 is unity-gain stable and has 60% lower voltage noise than the nearest competitor, while providing 110 dB PSRR to achieve designs for low noise preamps and gain staging.



APPLICATIONS

- Professional audio preamps
- ATE
- Imaging systems
- Medical instrumentation
- Precision detectors

AD8599 $3.20

The AD8599 provides the high output current necessary for robust low noise design and delivers a higher dynamic output range for data conversion. Each op amp delivers excellent dynamic response with a slew rate of 15 V/μs and 10 MHz unity-gain bandwidth. Providing a dual version in a single package also eases design challenges in terms of layout and performance parasitics due to external components. The device is available in an 8-lead SOIC.

- Low noise: 1 nV/√Hz p-p at 1 kHz, 120 nV p-p from 0.1 Hz to 1 Hz
- Low current noise: 3.5 pA/√Hz
- Low offset voltage: 100 μV max
- High drive current: 50 mA
- CMRR: 120 dB
- Slew rate: 15 V/μs
- Operation: ±5 V to ±15 V

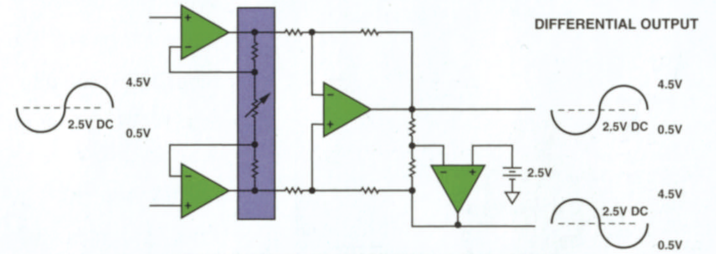
Zero-Drift, Digitally Gain-Programmable Instrumentation Amplifier Simplifies Instrumentation and Industrial Control Design

The AD8231 is a zero-drift, low voltage, rail-to-rail instrumentation amplifier with programmable binary gain levels from 1 to 128. An undedicated zero-drift output amplifier can be used for additional gain, multipole filtering, differential signal driving, or as an extra amplifier—offering additional flexibility, and simplifying your design. All gain setting resistors are internal, containing gain drift to 10 ppm/°C. The AD8231 offers low offset of 20 μV and input voltage offset drift of 50 nV/°C over the entire extended industrial temperature range of –40°C to +125°C. In addition, rail-to-rail output maximizes dynamic range. The AD8231 is available in a 16-lead, 4 mm × 4 mm LFCSP.

The versatile AD8231 is well-suited for operation with the AD7942, AD7685, AD7980 PulSAR® ADCs, the ADuC70xx precision analog microcontroller family, and the ADR121 precision micropower LDO voltage reference.

- Digitally programmable or pin strapped gain settings:
  - G = 1, 2, 4, 8, 16, 32, 64, and 128
- CMRR: 122 dB min @ 60 Hz, G = 128
- Bandwidth: –3 dB @ 1 MHz, G =1
- Input referred noise: 32 nV/√Hz
- Single-supply range: 3.3 V to 5 V
- Low shutdown power: 1 μA

DIFFERENTIAL OUTPUT INTERFACE WITH DIFFERENTIAL INPUT ADC



AD8231 $1.69

APPLICATIONS

- Pressure and strain transducers
- Thermocouplers
- Automotive diagnostics
- Gain and level-shifting circuits
- Zero-drift, multipole filters

Online seminar available on demand:
"In-Amps: How and When to Build Them" at *www.analog.com/onlineseminars*.

Inventory Code: AMPS-V7-IS1-07
Printed in the U.S.A.
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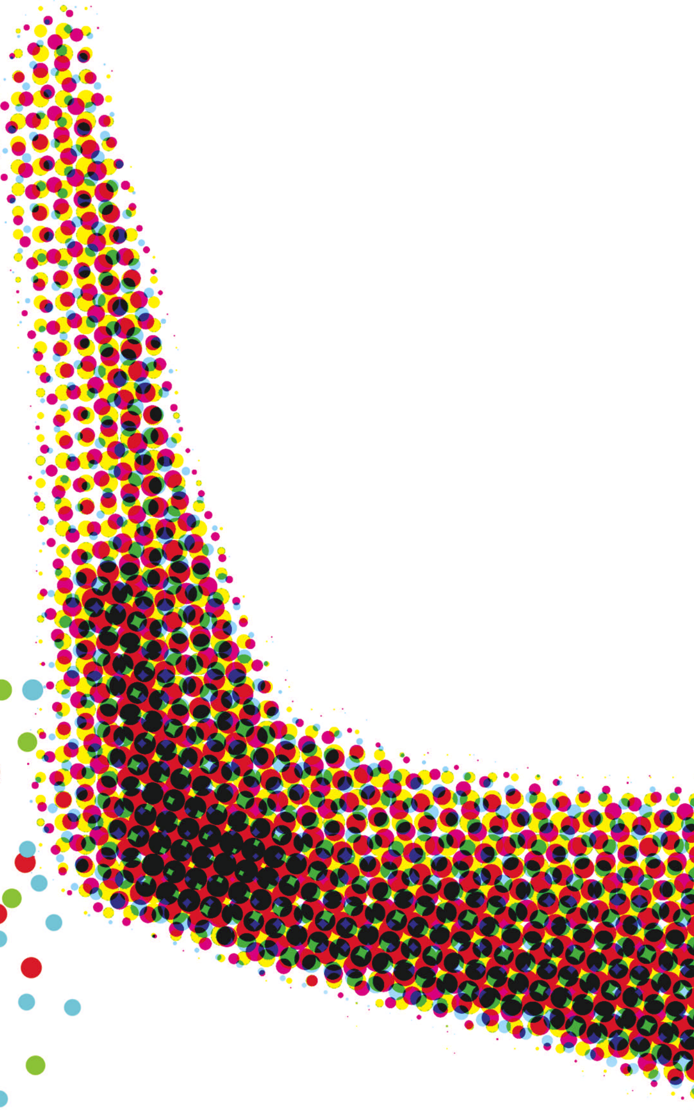
IMAGING BEYOND PIXELS:

enhancing the elementary picture



WITH PER-SENSOR PIXEL GROWTH SLOWING, HOW ELSE CAN DIGITAL-STILL-CAMERA MANUFACTURERS DIFFERENTIATE FROM EACH OTHER? HOW DOES THIS DIFFERENTIATION BRING THEM INTO GREATER COMPETITION WITH VIDEOCAMERAS? TO WHAT DEGREE WILL CAMERA PHONES SUPPLANT THEM BOTH? AND WHERE WILL SENSOR SUPPLIERS TURN TO CONTINUE FILLING THEIR FABS?

BY BRIAN DIPERT • SENIOR TECHNICAL EDITOR

A 2004 *EDN* cover story made the then-somewhat-controversial claim that image sensors' pixel-count growth rate would soon slow and that sensor implementers would subsequently need to distinguish their system designs using other measures of image quality and capability (**Reference 1**). How did the prognostication pan out? Here's one case study: In mid-2004 when I was researching the article, 8M-pixel mainstream DSLRs (digital single-lens-reflex cameras) were ramping into production; 6M-pixel predecessors had appeared approximately one year earlier. Yet, it took roughly *2.5 years* for 10M-pixel models to subsequently emerge. A number of recent analyst reports also concur with *EDN*'s 2004 forecast, as did every company I contacted in researching this article.

EDN Executive Editor Ron Wilson focused one of his 2007 CES (Consumer Electronics Show) online reports on imaging, and, in it, he commented, "Today, it is arguable that the key differentiator in retail camera sales is still pixel count, even though this number has become about as relevant as, say, clock frequency in PC sales" (**Reference 2**). Wilson's analogy between the camera and PC businesses is apt for several reasons. AMD and Intel encountered well-documented leakage-current issues at the 90-nm-process step, which hindered both companies' abilities to increment their CPUs' clock speeds at historical rates. Also, consumers figured out that they no longer needed to upgrade their PCs to newer models at historic rates; their current systems, perhaps with a less costly hard-disk drive or memory midlife transplant, now delivered sufficient performance for several generations' worth of software upgrades and proliferations.

A decreased influx of consumer-tempting computer supply, coupled with decreased consumer demand for the supply that existed, has translated to the formation of a buyers' market. Nowadays, you can purchase a robust desktop PC for less than $500 and a full-featured laptop for only slightly more money—if any. Recently published statistics suggest a similar saturation of the DSC (digital-still-camera) market. Research company IDC, for example, reports that fourth-quarter-2006 DSC shipments dropped for the first time since the company began monitoring them; at 12.1 million units, they were 3% below the year-be-

AT A GLANCE

- A slowing rate of increase in image-sensor resolution clobbers camera prices and forces manufacturers to diversify their products' features.
- Revolutionary lens technologies decrease or eliminate the power consumption necessary for zoom and focus functions.
- Telescope-derivative optics slim the transparent material stack necessary to implement a given focal length or range.
- You've got no shortage of processing options at your disposal: generic DSP or imaging-tuned logic block, baseband or application processor, and dedicated IC or image sensor-enclosed. Selecting the correct candidate for your particular situation is a key challenge.
- Low-light sensors, new file formats, antishake techniques, and additional connectivity options are some of the factors that will define future cameras' feature proliferations.

fore figure (**Reference 3**). And, for all of 2006, IDC estimates, the US market grew by only 5%, notably lower than 2005's 21% growth, as well as below the company's previous prediction of 8% growth for 2006 (**Reference 4**).

IDC also reported that only approximately 15% of cameras sold in 2006 went to first-time DSC buyers, with the bulk of sales replacing or supplementing DSC owners' existing models. IDC expects zero growth in DSC shipments for 2007, with a decline beginning in 2008. Consumers are increasingly realizing that beyond 2 million to 3 million pixels of resolution, additional captured-image detail is largely wasted when printing out 4×6-in. pictures, even if they come from cropped versions of the original photos. Interestingly, Geoff Ballew, director of product marketing for handheld graphics processors at Nvidia, confirms this fact when he states that 2 million pixels are "great for 4×6-in. prints." This "ceiling" on resolution's meaningfulness is particularly evident when the camera has aggressively JPEG-compressed the source image. And, when consumers want to create a larger print, they may have also found that high-quality pixel interpolation within their computer's image-processing software often suffices. Camera manufacturers have predictably responded to waning demand by cutting prices. In researching this article, I collected numerous eyebrow-raising DSC prices, such as free-after-rebate, 3M-pixel cameras and 4M-, 5M-, 6M-, and 8M-pixel cameras for $50, $55, $91, and $100, respectively.

Granted, not all of these cameras came from name-brand manufacturers. And they offered elementary features: limited-to-nonexistent zoom ranges, for example, along with sketchy low-light performance. However, in the past, the specified resolution may have depended upon postcapture in-camera interpolation. In all of the current research's cases, on the other hand, the promoted specifications referenced the native resolution of the camera's integrated image sensor. And collapsing prices aren't restricted to point-and-shoot models; for example, the days of spending several thousand dollars for a low-end DSLR body are over. Instead, according to my researched pricing collection, an entry-level, 6M-pixel DSLR with an 18- to 55-mm zoom lens costs $400, an 8M-pixel DSLR with *two* lenses costs $700 ($500 with one lens), and 10M-pixel DSLR bodies sell for less than $800.

RETHINKING OPTICS

In assessing what features besides pixel count DSC manufacturers and their videocamera, camera-phone, and other competitors can harness to recapture consumers' wallets, begin by looking at the lens, within which an image's photons undergo their initial transformations. I'll concentrate on two key optics attributes: focus and focal length. Fixed-focus cameras, which some marketers alternatively call focus-free, have limited usefulness. They don't, for example, allow for arms-length self-portraits, and you can, therefore, find them only in the low-end market segments. And manual focus is a hassle, infeasible for users with poor eyesight, and incompatible with fast-moving subjects. These drawbacks are true even with motor-assisted—and

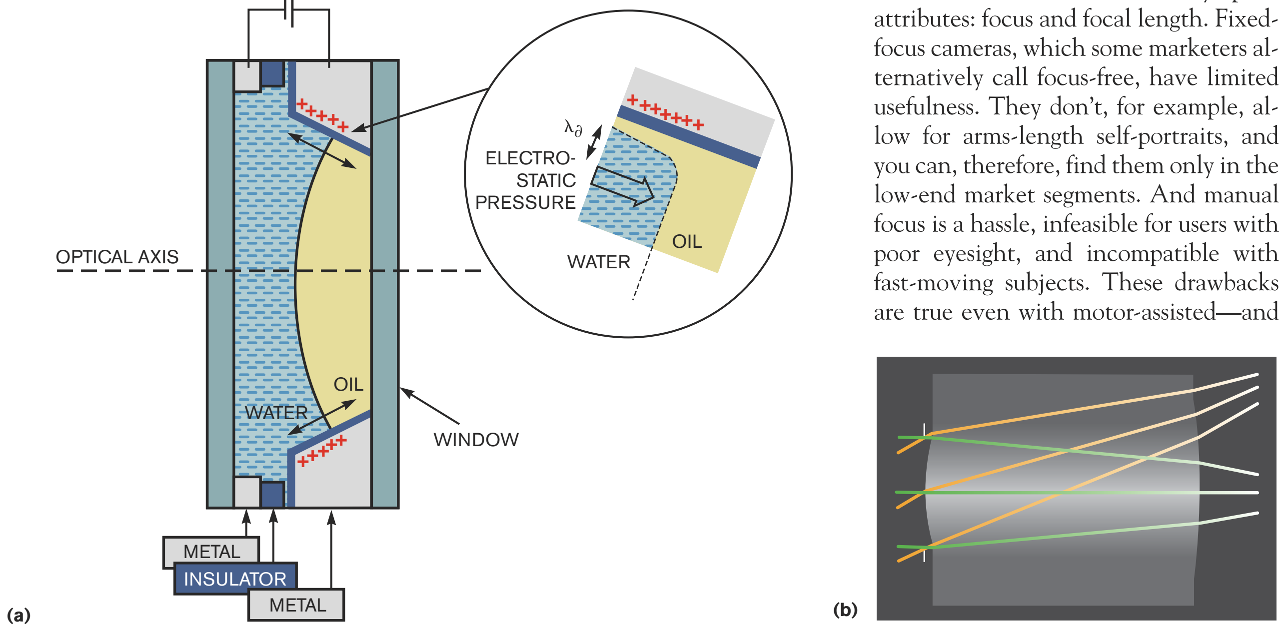


Figure 1 So-called liquid lenses implement focus and zoom functions with less power consumption than traditional motor-driven optics (a, courtesy Varioptic). Wavefront-coded lenses provide a compelling, albeit computationally intensive, no-focus path to extended depth of field (b, courtesy CDM Optics).

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- ISL6296

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- ISL59111

Core Power
- ISL6273
- ISL6274
- ISL9000
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Fuel Gauge
- ISL6295

Light Sensor
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thus incremental power-consuming—manual focus.

Yet, consumers are equally intolerant of autofocus cameras that select the incorrect focus plane in an image or that take too long to reach that point. “Stopping down” the lens to a smaller aperture—that is, a larger aperture value—and thereby increasing the depth of focus improve the likelihood of a sharp result. However, this technique also slows the shutter speed to the point that a user would be unable to hold a camera and still capture a sharp image in low-light settings. Using this technique would thereby require the use of additionally battery-draining, artificial-looking, and often insufficiently covering flash illumination.

Deep focus may also be incompatible with a user’s desire to intentionally blur the image foreground and background to draw viewers’ attention to the primary subject. So, instead or in addition, manufacturers are now throwing more processing horsepower at the problem. Modern cameras, particularly when users switch them to “portrait” modes, autodetect faces in the to-be-captured field of view and set both autofocus and autoexposure to optimize for them.

One emerging solution to the battery-sapping problem of motor-assisted focus, along with, for that matter, zoom, is liquid-lens technology. Companies, such as Varioptic, and research organizations, such as the IMRE (Institute of Materials Research and Engineering), are promoting this technology (see **sidebar** “Online addenda enhance the picture”). These lenses operate in a manner akin to that of the human eye, which is surrounded by muscles that subtly change its shape to alter its optics characteristics. Quoting from Varioptics’ technology overview: “The liquid lenses that we develop are based on the electrowetting phenomenon … a water drop is deposited on a substrate made of metal, covered by a thin insulating layer. The voltage applied to the substrate modifies the contact angle of the liquid drop. The liquid lens uses two isodensity liquids; one is an insulator, while the other is a conductor. The variation of voltage leads to a change of curvature of the liquid-liquid interface, which in turn leads to a change of the focal length of the lens” (**Reference 5** and **Figure 1**).

Alternatively, if deep focus is acceptable in your application, perhaps you’d be interested in a five- to 10-times increase in it without any requisite decrease in light transmission, such as that encountered when you stop down a lens aperture. In such a case, check out the wavefront-coding technology that OmniVision obtained when it acquired CDM Optics two years ago and now markets under the TrueFocus moniker. “Wavefront coding … offers systemwide optimization, whereby specialized optics, sensors, and signal processing work closely together to provide high-quality, low-cost imaging in spite of small package requirements,” claims CDM Optics’ co-founder and president, Edward Dowski, PhD. By shifting a higher percentage of the overall image-capture burden away from the optics and toward the image processor, you can also use wavefront-coding techniques to compensate for the dubious quality of low-cost plastic lenses as well as to counteract temperature and unit-to-unit manufacturing variability.

TrueFocus is, perhaps not surprisingly, a bundled package, integrating OmniVision-defined optics and OmniVision-designed image sensors, which have on-chip image processors. However, Product Manager Michael Hepp admits that other sensor and processor suppliers are developing conceptually similar approaches. Reflecting this fact, Ping Wah Wong, PhD, Nethra Imaging’s vice president and chief imaging scientist, notes, “Digital-focus technology that uses a form of predistortion with a specially designed lens and subsequently uses image processing to undo the distortion has shown to be promising because it can eliminate the autofocus mechanism in the lens.” Echoing Wong’s comments, Clay Dunsmore, chief technology officer for Texas Instruments’ Digital Camera Solutions group, notes, “Lenses can be made more compact by transferring quality requirements from the optical domain to the digital-image-processing domain. Examples include corner illumination and geometric distortion.”

Traditionally, two primary focal-length factors have contributed to optics bulk: a wide zoom range, versus a fixed focal length, and a long telephoto- or ultrawide-angle endpoint to that range. Yet, consumers wishing to pocket only a single camera desire a unit with as versatile as possible an optics subsystem, and, speaking of “pocket,” they’d also like the resultant camera to be neither too heavy nor too large. OmniVision’s Hepp notes that Motorola’s ultrathin Razr phone, a “once-in-a-lifetime” success story, has heavily influenced users’ expectations for all portable-electronics devices, especially in the United States. Unfortunately, supplemental wide-an-

ONLINE ADDENDA ENHANCE THE PICTURE

Invariably, some of the interesting information that I uncover during my research ends up on the cutting-room floor, at least from a print perspective, due to page-count limitations and other factors. Fortunately, though, the *EDN* Web site provides another publishing outlet, and, this time around, it’s particularly packed with material. “Form-factor transformations” predicts to what degree camera phones and still/videocamera hybrids will erode traditional DSC (digital-still-camera) dominance in the future, and “Application expansion” covers other uses for sensor suppliers’ wares. This article discusses some of the imaging breakthroughs that have emerged from academic- and industry-research projects; “Future forecasts” expands on the list.

More imaging news will come from mid-February’s 3GSM (Third Generation Groupe Spéciale Mobile) World Congress and this month’s PMA (Photo Marketing Association) shows; “Conference updates” will keep you abreast of all the breaking developments. “Education next steps” provides suggestions for further cultivating your imaging knowledge. And “Where in the world is Foveon?” documents my thoughts on this once-promising image-sensor start-up and shares a review of a book about the company. Visit the Brian’s Brain blog at www.edn.com/briansbrain for these and other relevant imaging postings.

Intersil Digital Light Sensors

High Performance Analog

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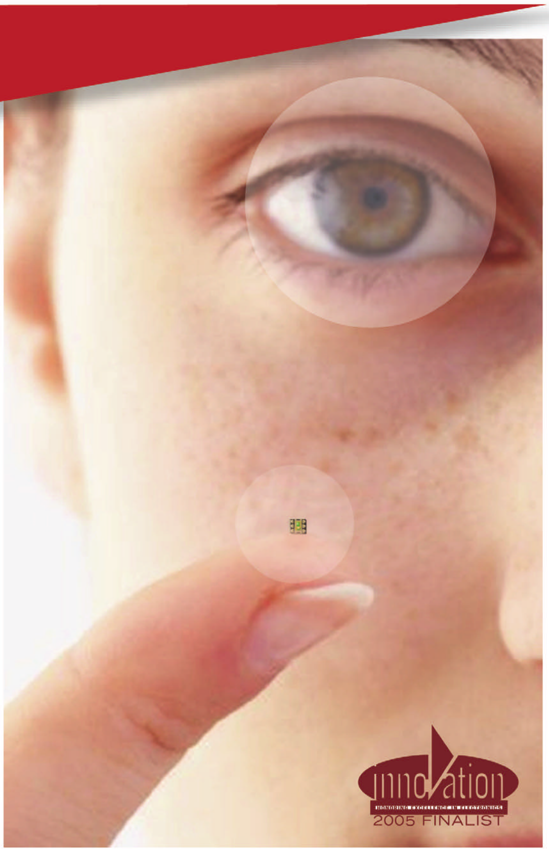
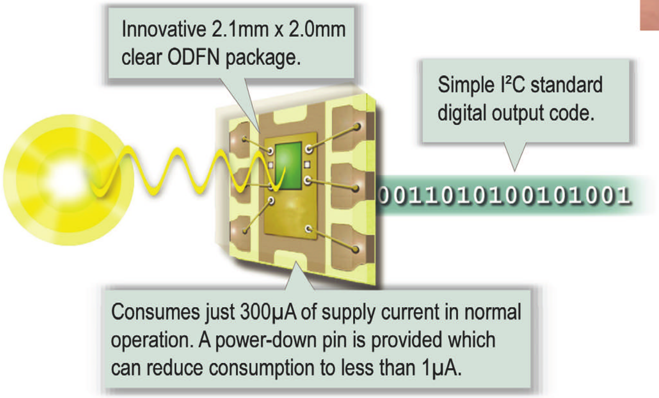


With light sensitivity only matched by the human eye, Intersil's ISL29001 Digital Light Sensor provides simple, pure 15-bit I²C digital data.

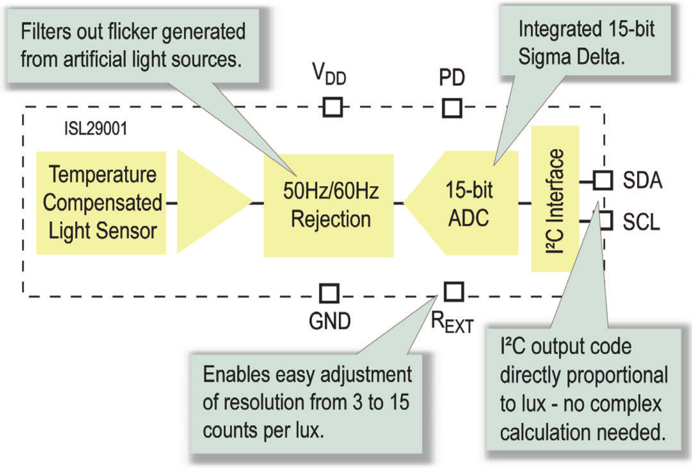
Drawing less than 300µA of supply current, the ISL29001 provides 15-bit effective resolution. This state-of-the art device integrates two photodiodes and an ADC into a super small 2.1mm x 2.0mm ODFN package. The digital data in standard I²C format couldn't be simpler to use. It's no wonder **EDN Magazine** has selected one of this family's light sensors as a finalist for this year's **Innovation of the Year Award**.



Innovative 2.1mm x 2.0mm clear ODFN package.

Simple I²C standard digital output code.

Consumes just 300µA of supply current in normal operation. A power-down pin is provided which can reduce consumption to less than 1µA.



Filters out flicker generated from artificial light sources.

Integrated 15-bit Sigma Delta.

Enables easy adjustment of resolution from 3 to 15 counts per lux.

I²C output code directly proportional to lux - no complex calculation needed.

ISL29001 Key Features:

- I²C interface produces simple I²C output code, directly proportional to lux
- 0.3 lux to 10,000 lux range
- 50Hz/60Hz rejection to eliminate artificial light flicker
- Human eye response
- 15-bit effective resolution
- Adjustable resolution: 3 to 15 counts per lux
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gle and telephoto lenses that, like a filter, screw onto the front of the primary optic haven't been largely successful for a variety of reasons, including inconvenience, added cost, and degraded quality. And the so-called digital-zoom—that is, pixel-interpolation feature—is thankfully fading from prominence; although it's arguably better than no zoom at all, its quality results are subpar, especially in the fast-capture-expectation and, therefore, limited-processing environment of a still or videocamera.

A tall order? No doubt. But several techniques can help address the seemingly divergent customer requests. Kodak's EasyShare V705 tackles the optics problem with two lenses and two 7.1 million-pixel sensors—a 23-mm, 35-mm-equivalent ultrawide-angle fixed lens and a 39- to 117-mm zoom lens (**Figure 2**). For another example of the range-versus-reach trade-off, look at Kodak's P712 and P880 Performance Series cameras, which have similar form factors. The P712 includes a 12× optical zoom, in a 36- to 432-mm focal-length range. Conversely, whereas the P880 offers "only" a 5× optical zoom, its reach extends from 140 mm all the way down to an ultrawide, 24-mm focal length.

Taking optics developments to a more revolutionary level, researchers at the University of California—San Diego recently unveiled an "origami" lens, which they based on reflective-mirror techniques that astronomical telescopes use but built on a single 5-mm disc of calcium fluoride. It promises to reduce the camera thickness required to implement a given focal length and focus range. "Traditional camera lenses are typically made up of many different lens elements that work together to provide a sharp, high-quality image. Here, we did much the same thing, but the elements are folded on top of one another to reduce the thickness of the optic," says Eric Tremblay, an electrical- and computer-engineering doctoral candidate at UCSD's Jacobs School of Engineering, in the university's newsletter (**Reference 6**). The initial prototype eightfold imager, which implements a 38-mm focal length and focuses on objects 2.5m away, was at least one-seventh the thickness of a conventional multielement lens cluster.

PROCESSING PIXELS

I asked Stuart Boyd, Analog Devices' product-line director for the company's high-speed-signal-processing group to provide an overview of the imaging businesses in which Analog Devices participates. "We're seeing manufacturers place more effort into helping their customers take better pictures. This [effort] is showing up in … face-detection-assisted autofocus and exposure, in-camera image correction at the push of a button, assistance in stitching shots together for panorama shots—stuff that used to be possible only in software that few of us bothered to deal with. What's happening inside the camera 'engine' is getting a lot more complex to manage and ensure [that] performance is fast enough to give the immediate results we all expect." Speaking of consumers who inappropriately judge their photographs against professionals' work in magazines, *EDN*'s Wilson echoes Boyd's observations: "This puts pressure on the camera architects to cram as much image quality into the acquisition process and as much postprocessing capability into the platform, as possible," he wrote in his online CES report.

Let's be clear: This problem is a *good* one for a processor vendor to have, and

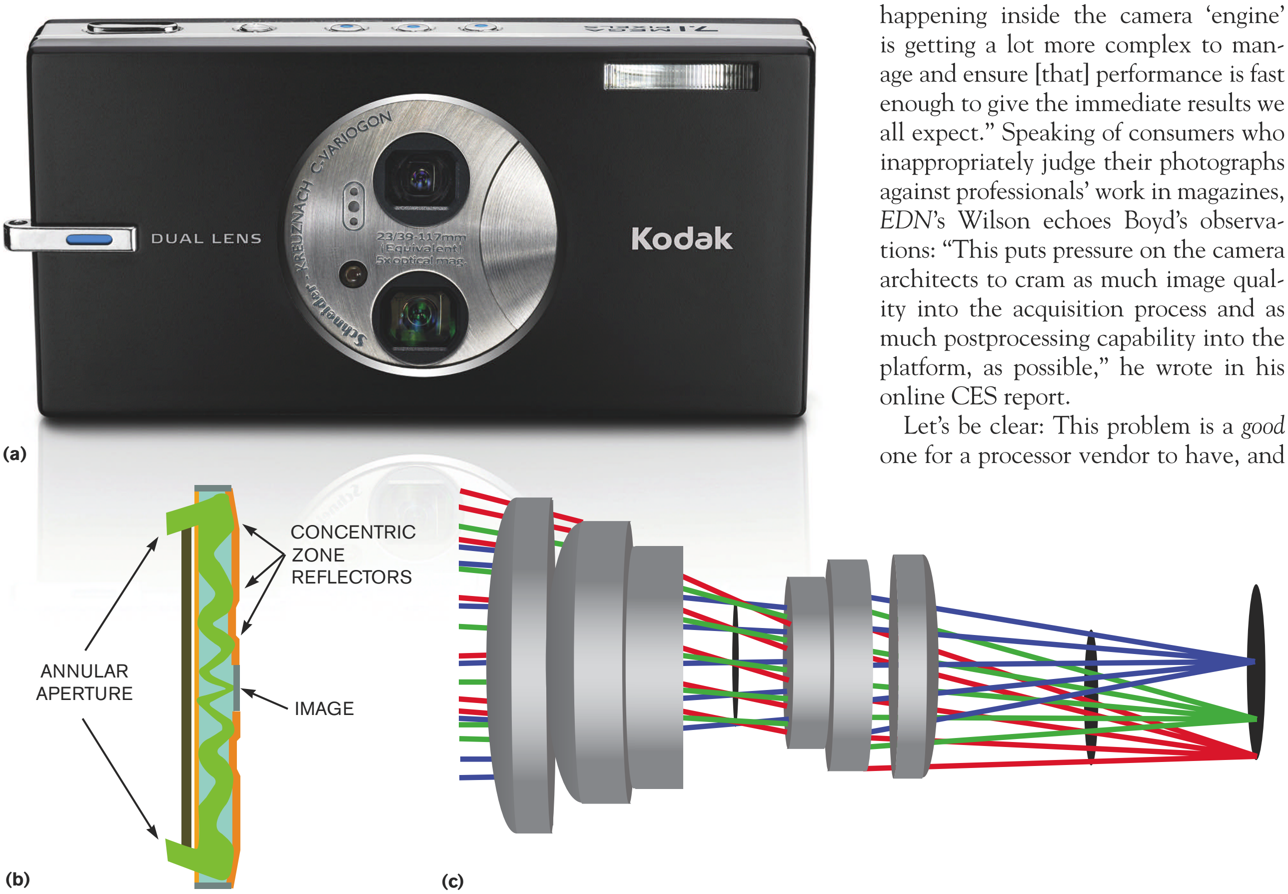

Figure 2 Kodak's EasyShare V705 harnesses dual lenses and dual image sensors to sveltely extend its optical range (a), and the University of California–San Diego's "origami" lens harnesses mirror-telescope-derived technology to the same end (b), versus a bulkier traditional multielement lens stack (c).

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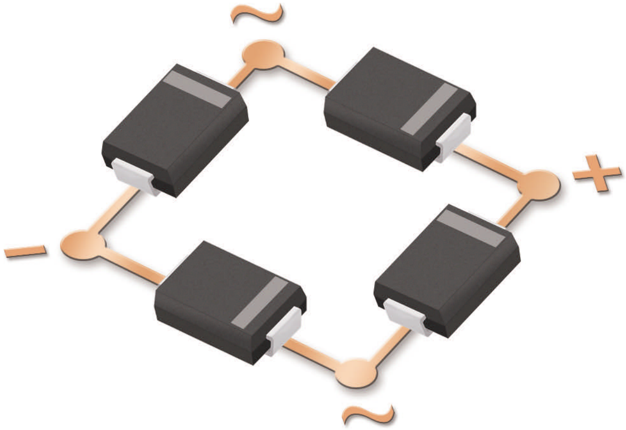

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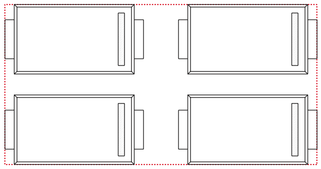

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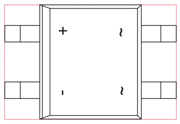

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it shows no sign of disappearing any time soon. But which processor vendor and which architecture are optimal for your next system design? *This* problem has no easy answer; when researching alternatives, you'll face a spectrum of offerings—from hard-wired to fully software-programmable. NuCore Technology's processors' imaging-centric pipelines inhabit the hardware region of the spectrum, with Texas Instruments' DSC processors' combination of a generic DSP core and imaging-centric peripherals on the opposite, software-centric side. (Note that both NuCore's and TI's products embed an ARM core as the overall system processor.) Reflecting TI's image-processing approach, Kanika Ferrell, marketing manager for the digital-camera group, comments, “Because multiple functions are being run on a single core, it requires that the image processor in the system have enough horsepower to run multiple functions simultaneously. … To keep power consumption low, manufacturers move to more advanced process-technology nodes and run the processor at higher speeds while using lower power to do so.”

Nvidia's Ballew, on the other hand, suggests some image-processing areas in which dedicated-hardware support makes particularly good sense:

- **“A very fast datapath into the GPU** [graphics-processing unit]. Benefit: Very fast click to capture; the sensor module can be set in full resolution for preview so there is no delay resetting the sensor from a low-resolution preview to full-resolution capture.
- **“Real-time-JPEG encode**. Benefit: Rapid multishot; the image can be compressed as fast as the sensor sends the data, so the user can capture several frames in a row with a single click of the shutter release. This [feature] helps to capture action shots or those hard-to-catch photos. Real-time JPEG also reduces memory requirements, so it helps OEMs make affordable phones. … And full hardware JPEG encode and decode reduce the power required to compress and decompress images.
- **“ISP** [image-signal processor]. Benefit: The ISP is key for autofocus, auto-white balance, and auto exposure and the variety of image features, such as sepia, black and white, antique, red-eye reduction, and edge sharpening. It also gives the phone OEM more flexibility to choose camera modules with or without an ISP. The newest sensors typically come to market without an ISP integrated. Putting this function into the graphics processor saves cost and board space compared to an external ISP. This [feature] also reduces the power required compared to software-based ISPs.”

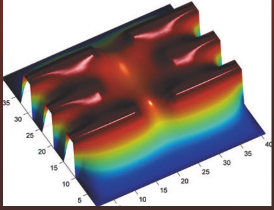
ALL OF THE VARIOUS IMAGE-PROCESSING APPROACHES HAVE STRENGTHS AND SHORTCOMINGS.

On that last point, given that one of the long-touted advantages of a migration from CCDs (charge-coupled devices) to CMOS sensors is the ability to include image-processing logic alongside the sensor array, you might predict that the CMOS-sensor suppliers wouldn't necessarily agree with Nvidia's partitioning stance, and you'd be right. The latest generation of ISP-inclusive sensors even incorporates support for the JPEG-encoding function. Andrew Burt, vice president of Toshiba's ASSP (application-specific-standard-product) business unit's imaging- and communications-marketing group, comments, “There is continuing debate about whether the ISP should be integrated on the CMOS-image-sensor die or onboard the baseband processor. Many handset manufacturers tell us that a CMOS-image-sensor SOC [system on chip] with an embedded highly optimized ISP is preferable. It offers system benefits that leverage the CMOS-image-sensor designer's in-depth knowledge. This [benefit] becomes key as resolutions approach 5M pixels and beyond. However, even at 2M pixels, an SOC approach can provide end users with a better visual experience.” In reality, all of the various image-processing approaches have strengths and shortcomings. To guide your selection, assess factors such as cost, performance, degree of integration, power consumption, flexibility versus the flexibility requirements of your application, and development-tool maturity and robustness.

One increasingly key camera feature that all the companies I interviewed for this article mention is the need to deliver increasingly high-quality images at increasingly low-ambient-light levels. Said a different way, they point out the need for the camera to operate at ever-higher shutter speeds for a given subject illumination strength, thereby obviating the need for battery-draining flash operation and acting as a first-pass image-stabilization scheme. This consumer demand flies in the face of the fact that, as sensors' pixel pitch decreases, each pixel's photodiode captures fewer photons in a given amount of time, thereby inherently decreasing the photodiode's light sensitivity.

It is essential to accomplish this high ISO (International Organization for Standardization)-processing trick with low image noise, because noise directly impacts compression efficiency, and the smaller the JPEG file, the more pictures a consumer can take before filling up a flash-memory card or another storage device. (ISO 5800:1987 describes photographic film's or a sensor's sensitivity to light, also known as its “speed” and often also called its ISO number.) Nvidia, for example, has branded its proprietary JPEG scheme with the Fotopak marketing moniker. And NuCore's two-chip CleanCapture approach, which works in conjunction with CCDs, does as much image processing as possible in the analog domain with its NDX chips before passing on the data to a digital-domain SiP companion processor. (CMOS-sensor-based designs don't use the company's front-end analog processor.) Evolutionary sensor improvements can help to some degree; for example, Toshiba's Burt notes that the company is “working on new conformal-microlens technology that provides a gapless microlens with increased light-gathering efficiency instead of today's circular microlenses that can't cover the entire pixel area of the image-sensor array.”

Perhaps, though, the industry needs a more fundamental breakthrough in image-sensor design to fully address consumers' low-light-with-high-quality contradictory expectations. At both this year's and last year's CES, Planet82, a small company and partner of the Nano Scale Quantum Devices Research Center of the Korea Electronics Institute, showcased the ability to capture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discernible, albeit fuzzy, images—both still and low-frame-rate video and both black-and-white and color—of objects at *extremely* low ambient-light levels. I attended a demonstration at this year's show and was impressed by the company's achievement. Granted, the sensor was low-resolution—that is, VGA—although the company expects a 2M-pixel sensor to be out of fab by the time you read this. Also, the technology's cost, manufacturing yield, stability through operating lifetime and extremes of voltage and temperature are all currently unknown.

"Planet82's new VGA-color SMPD [single-carrier modulation-photo detector] is the … first, full-color, high-sensitive imaging chip for taking pictures or video in the dark without a flash," says Hoon Kim, PhD, chief technology officer for Planet82. "SMPD combines the clear-image quality, high sensitivity, and wide dynamic range of existing imaging technology with powerful nanotechnology, making it 2000 times more light-sensitive and 50% smaller than traditional CMOS and CCD sensors. … Unlike photodiode-based CMOS and CCD technologies, which require millions of photoelectrons per pixel unit to create an image, the SMPD is able to react to tiny amounts of photons in light levels less than 1 lux, the equivalent of the light from one candle a meter away."

Planet82 remains tightlipped about the specifics of its nanotech accomplishment, but, according to a report by MicroDesign Resources' Max Baron in April 2006, "Planet82 seems to base its development of nanotechnology on SMPD pixels that can deliver high amplification (high electron yield) by creating a semiconductor 3-D confinement smaller … than the de Broglie wavelength. [The de Broglie hypothesis states that all matter has a wavelike nature, **Reference** 7.] The mechanism of translation of light energy into charge for available CCD and CMOS devices is based on the conversion (subject to efficiency) of one photon to one electron. The SMPD uses the same mechanism, but the electron created is amplified by quantum effects, generating several thousands of electrons. CCD and CMOS devices use a PN-junction photodiode to provide the photoelectrical transformation. The detection mechanism employed by the SMPD is fundamentally different: the SMPD implements artificially made potential barriers in every electrical energy band of interest. A few injected photons will find it easy to lower the barrier, allowing the structure to generate a significant electrical charge" (**Reference** 8).

FEATURE INFLATION

Sometimes, the two-step scheme of simply cranking up the signal gain coming off an image sensor and then processing out the consequent noise is insufficient for stabilizing images. For example, Nethra's Wong points out, "Camera shake can happen easily in cell-phone cameras because of the small form factor and because the camera is usually operated with one hand." In such cases, more elaborate image processing is necessary. Electronic stabilization incorporates an oversized image sensor. The processor identifies the pixel locations of high-contrast images, and, if they move from one frame to another, it compensates by proportionally shifting the captured image—as long as the entire scene still fits within the sensor's boundaries. Even more elaborate image-stabilization schemes involve electromechanical techniques that shift either the image sensor or the lens elements in response to an accelerometer-sensed jostling of the camera.

It might be easy to conclude that smaller pixel pitch is overwhelmingly a bad thing for imaging. That supposition would be premature, however. Applications that beg for ultrahigh resolution do exist. Ask Hasselblad, for example, which just unveiled the $24,995, 31M-pixel H3D-31 camera, which represents a step *backward* from last year's 39M-

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pixel model. Or ask Canon, which, according to rumors, is developing a 22M-pixel DSLR. Alternatively, think of what else you could do with all those pixels, besides devoting them to resultant image pixels on a 1-to-1 basis.

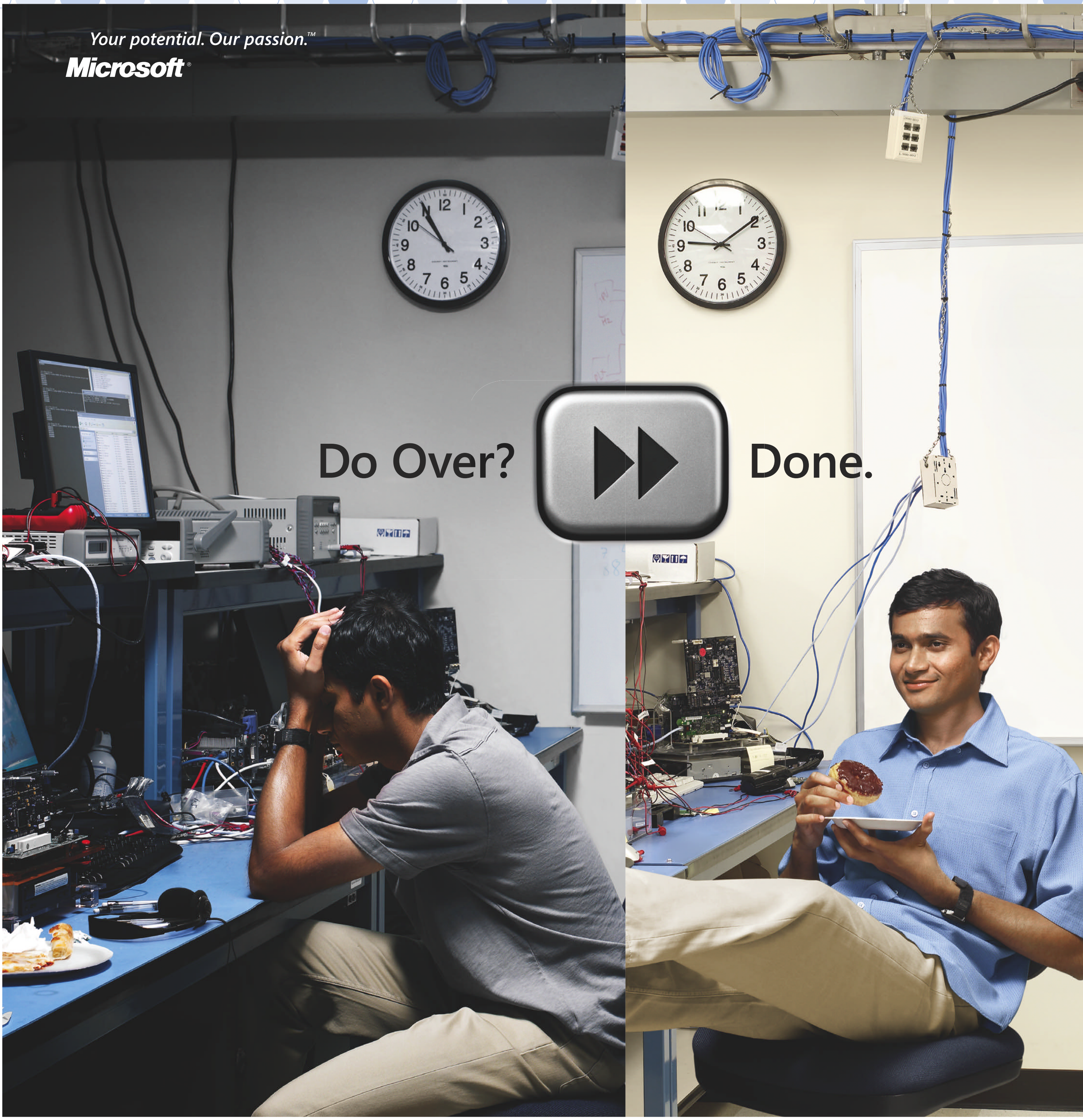
Most modern cameras, with the exception of prism-based, three-sensor configurations or those derived from Foveon's three-photodetector-per-pixel-sensor approach, embed sensors that include a multicolor-filter array ahead of the photodetector array. Common filter matrices include the Bayer pattern, which contains twice as many green filters as either red or blue; the Sony-developed RGBE (red/green/blue/emerald) Bayer enhancement, which adds an emerald-green filter; and the CYGM (cyan/yellow/green/magenta) filter array. Regardless of the raw image's filtered state, postcapture interpolation derives red, green, and blue values for each pixel. Instead, though, why not harness burgeoning image-sensor-native resolutions to dedicate red-, green-, and blue-filtered sensor subpixels to each corresponding image pixel?

You can also harness the multiple-sensor-pixel-per-image technique to expand the dynamic range of the resulting image. Today, photographers who desire to generate HDR (high-dynamic-range) pictures take underexposed, overexposed, and correctly exposed shots of the same scene and then combine them in a computer using Adobe Photoshop or a similar program. This approach is not only incompatible with moving subjects, but also cumbersome and time-consuming. Instead, by placing a variable neutral-density filter array ahead of the sensor or by designing sensor subpixels with varying photon-integration characteristics, you can accomplish a similar result in the camera and with only a single shot.

Unfortunately, the more-than-10-year-old JPEG format, which still dominates in still-image-capture applications, has outmoded characteristics that hinder imaging advancements, such as HDR. It supports only 24-bit-per-pixel, or 8-bit-per-color-per-pixel, maximum dynamic range, and the more flexible JPEG 2000 approach hasn't achieved widespread adoption. Microsoft's Windows Vista OS and the company's latest generation imaging applications robustly support its Windows Media Video-derived HD Photo format, and, with it, the company hopes to break the JPEG bottleneck on imaging innovation. Key HD Photo attributes, according to Principal Product Manager Bill Crow, include 2× compression efficiency versus JPEG for typical photographic content; a lossless-compression option, which typically provides 2.5× compression; significantly higher color fidelity at any compression ratio, which the company primarily accomplished through the use of 4:4:4 or 4:2:2 chroma sampling; fewer additive artifacts with multiple recompressions; support for many more pixel formats, including gray scale, CMYK, and N-channel; and support for 8 to 32 bits per color, integer and fixed- and floating-point formats, HDR, and wide-gamut images.

"HD Photo uses a biorthogonal lapped transform, combined with advanced entropy coding, a high-performance, reversible color-space transform, and numerous other innovations," says Crow. "The core transform is functionally equivalent to the DCT [discrete-cosine transform] in JPEG. HD Photo's algorithm is incrementally more complex to support the innovations that significantly improve compression efficiency, but this additional processing does not require complex operations or instructions. All processing involves simple integer math, which can be easily accelerated with parallelization, pipelining, [or both]. HD Photo encoding and decoding is based on macro blocks, enabling progressive image encoding and decoding using a minimal memory footprint. For a typical camera-encoding application, the target memory-buffer requirement is 18 pixel rows.

"While HD Photo's compression algorithm is incrementally more complex than JPEG, the improved compression efficiency results in smaller compressed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bit streams, reducing the total processing required. Most important, this [approach] reduces the amount of variable-bit-length processing, which is the portion of the overall algorithm that is least able to be accelerated." A DPK (device-porting kit) is currently available in a 100%-royalty-free fashion for building support for HD Photo into an imaging application. It includes a bitstream specification, reference ANSI C source code for the encoder and decoder, and sample applications, and it supports both little- and big-endian processor architectures. Microsoft also plans to deliver a Quicktime codec for Apple's OS X.

According to TI's Ferrell, "Camera features are beginning to normalize. We aren't seeing many 'new' features on cameras but rather improvements in the existing features, such as improved response time and faster processing of the advanced features already integrated into the system." Although Ferrell's perspective may be accurate in the broad sense, plenty of examples exist of cameras that make more radical feature transformations in attempting to tempt both DSC owners to upgrade and those on the fence to take the first-time DSC plunge.

CES is a prime opportunity for vendors to unveil their latest image-capture ideas. New products include GoPro's Digital Hero 3 for extreme-sports fanatics, which straps to a user's wrist and captures either bursts of 3M-pixel images or as much as 54 minutes of 30-frame/sec video with sound. The 4.5-oz unit is waterproof to 100 feet and has a manufacturer's suggested retail price of $139.99. Kodak unveiled its 4M-pixel EasyShare-One at the 2005 CES. It contains a Wi-Fi transceiver that enables you to wirelessly e-mail, print, and upload photos to your PC, as well as to directly access Kodak's online-storage service. Cameras from numerous suppliers now contain Bluetooth connectivity for printing and photo transfer, supplementing traditional wired-USB links. UWB (ultrawideband)-silicon vendors are eyeing this same application as a future opportunity. Another unit, Samsung's 7M-pixel VLUU i70, includes HSDPA (high-speed-downlink-packet-access) cellular-data connectivity, along with text-messaging functions. Sanyo's Xacti HD2 hybrid high-definition still/videocamera embeds an HDMI (high-definition-multimedia-interface) transmitter for directly tethering a display. Ricoh's 8M-pixel 500SE, like several other cameras now available, integrates a GPS (global-positioning-system) module that enables users to record the location where they took a picture. Some camera phones mimic this capability, albeit with a lower degree of accuracy, through cellular-tower triangulation. **EDN**

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Board standards seek THE HOLY

AS EXPECTATIONS FOR EMBEDDED SYSTEMS SOAR, STANDARDS ORGANIZATIONS ARE SCRAMBLING TO OFFER DESIGNERS THE BEST COMBINATION OF COST, SIZE, RELIABILITY, AND PERFORMANCE.

Restricted budgets and shortened schedules have forced design teams to eschew proprietary designs and adopt open standards for low- to medium-quantity, high-performance embedded projects, such as medical instrumentation, military systems, communications installations, and process automation. Their challenge is to select a standard that can deliver the performance, form factor, and cost necessary for the current project and offer ample expansion for expected updates to data rates and processing requirements. Today's board-level standards include names such as VMEbus, PCI, CompactPCI, PC/104, and AdvancedTCA (Advanced Telecom Computing Architecture), plus a variety of stand-alone modules and daughtercards. Each standard targets a different group of users and receives support from an industry group responsible for changes and extensions necessary to keep the specifications viable as performance expectations advance.

Embedded-system designers rely on open standards to ensure an ample selection of pre-engineered, off-the-shelf system components to satisfy at least some of the requirements of each new project. Open standards allow designers to purchase components from any number of vendors and ensure hardware and software interoperability. Standards-based system enclosures, processor cards, peripherals, and off-the-shelf user interfaces may reduce a typical embedded-system project to little or no hardware design and the application-specific software. Industry standards ease the software-development effort by providing access to compatible operating systems, vendor-supplied drivers, and sample source code. Board standards also eliminate the trial-and-error design iterations necessary to get the best cooling performance and mechanical alignment.

Although board standards try to appeal to a large segment of the embedded-system industry, inherent problems exist in the specification-development and -ap-

GRAIL

BY WARREN WEBB • TECHNICAL EDITOR

proval process. In general, standards organizations are slow to respond to technology advances, because they must wait for a consensus of their members before finalizing updates. Yet, if they attempt to keep up with early changes, the number of options confuses the industry and reduces the probability of interoperable products. For example, the AdvancedTCA standard has several alternatives for serial data exchange, including Ethernet, Fibre Channel, InfiniBand, StarFabric, PCIe (PCI Express), and RapidIO. Although some board vendors have developed unique designs to accommodate multiple options, the failure of the industry to settle on one or two switched-fabric technologies is a possible flaw in the continued success of COTS (commercial-off-the-shelf) products.

GOLDEN OLDIES

Standards organizations must also face the issue of legacy compatibility when upgrading or extending the performance level of board specifications. Designers want a large selection of compatible boards, but a major upgrade to the standard could render a large segment of products inoperable with new hardware. In general, most standards allow you to locate both old and new technologies in the same system with nonoverlapping card-edge connectors or special backplanes that provide each version a few slots. For example, the VMEbus standard is the oldest of the current embedded-system architectures, yet most of the first products are still compatible with the latest products. Standards must also address long-term availability, a prime requirement for high-performance embedded products. Although the average life of desktop components is about 18 months, users expect typical embedded products to remain in service for five years or more.

CompactPCI also has a history of updates in search of the right combination of features to satisfy much of the embedded-system community. CompactPCI packages low-cost, PCI-based desktop hardware into a rugged form factor, giving embedded-system developers access to off-the-shelf silicon and desktop software applications. The PICMG (PCI Industrial Computer Manufacturers Group) controls the CompactPCI specification, which it bases on the Eurocard industry standard defining both 3U and 6U board sizes. The more popular 6U version has as many as five connectors on the rear of the card, allocating two for the CompactPCI bus and the remaining three for optional user-defined I/O connections. Through a series of updates for high-performance applications, PICMG has extended the CompactPCI specification to include a packet-switching backplane that adds dual-switched 10/100/1000 Ethernet fabrics to the user-defined pins.

AT A GLANCE

- Standards organizations must constantly update board specifications to enable an ample supply of pre-engineered, off-the-shelf products for embedded-system designers.
- Multiple serial-communications options in board-level specifications can lead to industry fragmentation and product-interoperability issues.
- CompactPCI Express uses silicon and software from the desktop to enable a high-performance, rugged, yet low-cost embedded-system architecture.
- AdvancedMC modules serve as mezzanine cards for AdvancedTCA and plug directly into the backplane for the new MicroTCA system standard.

More recently, PICMG followed the lead of desktop technology and incorporated PCIe into the CompactPCI specification. CompactPCI Express offers scalable high-bandwidth datapaths, packetized data protocols, and compatibility with PCI hardware and driver software. The basic PCIe link comprises two signal paths that use LVDS (low-voltage differential signaling) and constant-current line drivers to communicate at 5 Gbps in each direction. You can increase the bandwidth of an individual PCIe link by simply adding signal pairs, or "lanes," until you reach the desired performance level. MEN Micro offers a 3U CompactPCI Express single-board computer that features the Intel 2.16-GHz Core 2 Duo processor (**Figure 1**). Highlighting Intel's Mobile 945GM Express chip set, MEN Micro's F17 includes six PCIe lanes as well as two SATA (Serial Advanced Technology Attachment) lines. The board's memory complement comprises 4 Mbytes of L2 cache integrated into the Core 2 Duo and as much as 4 Gbytes of fast DDR2 DRAM. Standard I/O on the front panel includes a VGA connector, two Gigabit Ethernet interfaces connected using PCIe, and two USB 2.0 ports. Because it employs components from Intel's embedded-system line, the F17 has a guaranteed minimum standard availability of five years. MEN

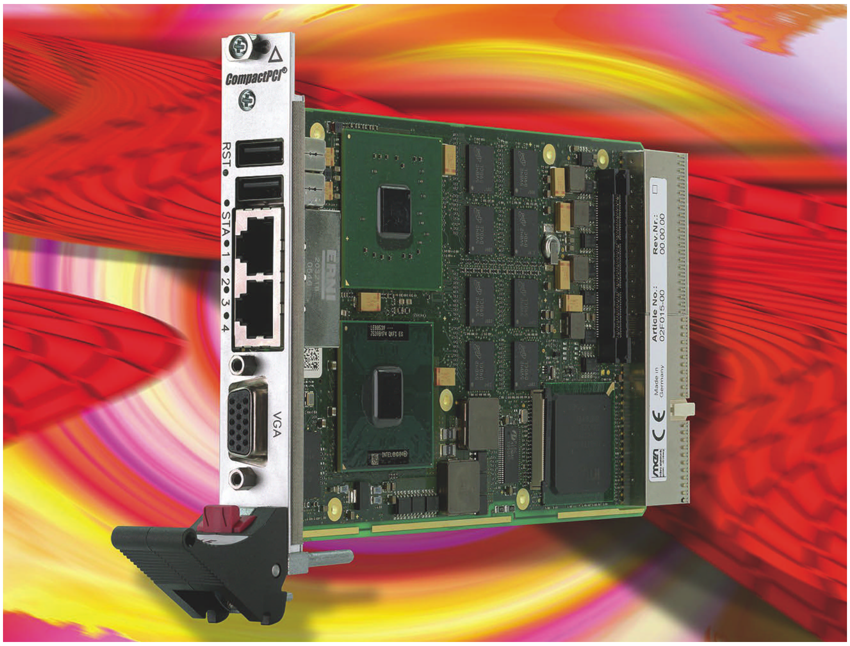

Figure 1 Conforming to the CompactPCI Express standard, MEN Micro offers a 3U single-board computer that features the Intel 2.16-GHz Core 2 Duo processor.

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DAC082S085	8-bit	2	3 µsec	MSOP-10, LLP-10
DAC102S085	10-bit	2	4.5 µsec	MSOP-10, LLP-10
DAC122S085	12-bit	2	6 µsec	MSOP-10, LLP-10
DAC084S085	8-bit	4	3 µsec	MSOP-10, LLP-10
DAC104S085	10-bit	4	4.5 µsec	MSOP-10, LLP-10
DAC124S085	12-bit	4	6 µsec	MSOP-10, LLP-10

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Micro provides board-support packages for Windows, Linux, VxWorks, and QNX. The price for the F17 is $2920.

SCRATCH START

Another approach to finding the perfect architecture for a range of applications is to start from scratch and create a new specification, basing it on the latest technology without regard for legacy products. For example, the AdvancedTCA, which debuted in 2003, created an entirely new set of board, backplane, and software specifications for the next generation of telecom equipment. With a larger form factor, high-availability features, and high-speed fabric interconnections, AdvancedTCA promised to be a viable off-the-shelf alternative to the proprietary equipment prevalent in the telecom industry. The AdvancedTCA specification provides hot-swap capability for all boards and active modules, allowing systems to achieve and even exceed the elusive "five-nines" availability (99.999%). The fabric interface provides a full mesh interconnection, in which each slot has a direct connection to every other slot.

For maximum versatility with high-performance applications, AdvancedTCA designers added replaceable plug-in modules or daughtercards with many of the same features as the base architecture. The resulting AdvancedMC (Advanced Mezzanine Card) standard of-

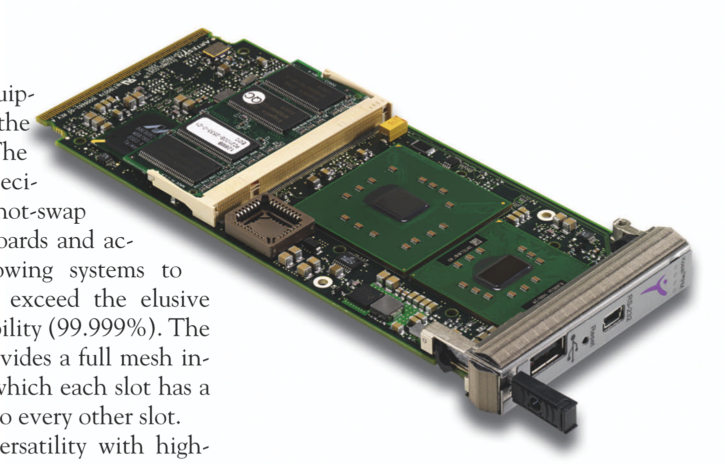

Figure 2 The KosaiPM is an AdvancedMC processor module featuring hot-swap capability and both PCI Express and dual Gigabit Ethernet interfaces.

STACKABLES SEEK A NEW DIRECTION

Board standards either transform themselves to adapt to the latest system requirements or fade into obscurity, like the S-100 bus or Multibus. The PC/104 standard has been struggling of late to deal with the end of ISA-bus silicon. Although the PC/104 Consortium has updated the standard to include the PCI bus (PC/104-Plus) and then to omit the ISA bus (PCI-104), most off-the-shelf boards still require the ISA signals to operate. PC/104 is popular among embedded-system designers because it requires no backplane and allows modules to stack like building blocks. Mounting holes in the corner of each 3.55×3.775-in. module allow you to fasten the boards to each other with standoffs.

Micro/sys, a long-time PC/104 vendor, recently started a campaign to create an entirely new stackable architecture, borrowing the form factor from PC/104. The new architecture uses a more modern communications protocol, USB, but retains the size and stacking advantages of PC/104. StackableUSB supports as many as 16 peripheral boards, takes advantage of USB plug-and-play features, and eliminates the cable with a built-in stack-through connector. To encourage support from a variety of vendors, Micro/sys has already announced a CPU board and a general-purpose I/O card. The USB148 I/O module (Figure A) delivers 48 digital TTL I/O lines plus three 16-bit timer/counters. All discrete I/O lines have software-programmable pullups or pulldowns. The core of the USB148 is a 8051-compatible microcontroller unit that runs at 48 MHz and integrates many peripherals, such as the 10-bit A/D converter, two UARTs, and others that are available to users. Micro/sys provides a predefined protocol that carries data over the USB, so there is no need for users to develop code for microcontroller. The USB148 starts at $125 (one). You can follow the progress of the StackableUSB standard at www.stackableusb.com.

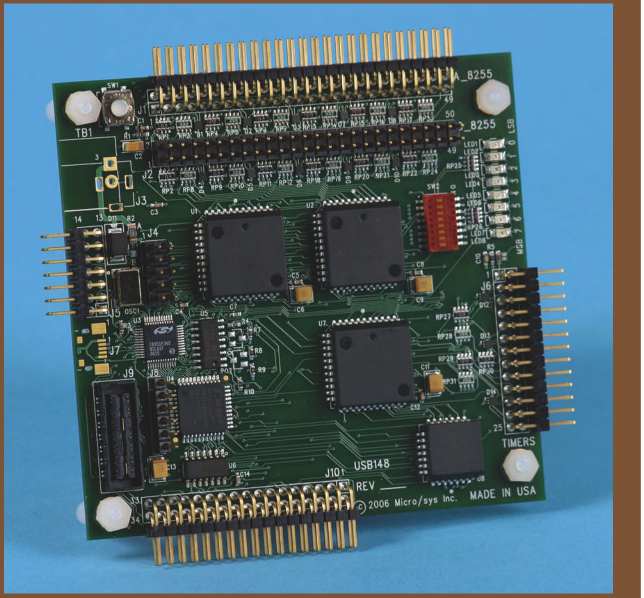

Figure A Although the industry has not yet approved it as a standard, the StackableUSB I/O module from Micro/sys includes 48 digital TTL I/O lines plus three timer/counters.

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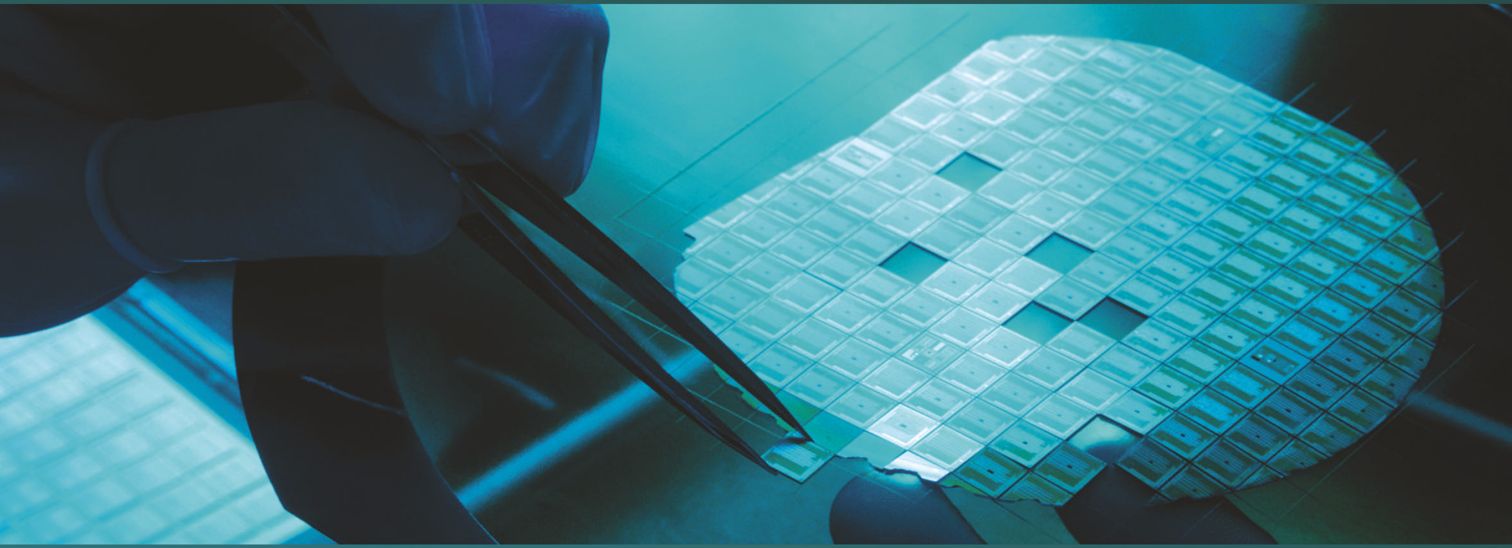

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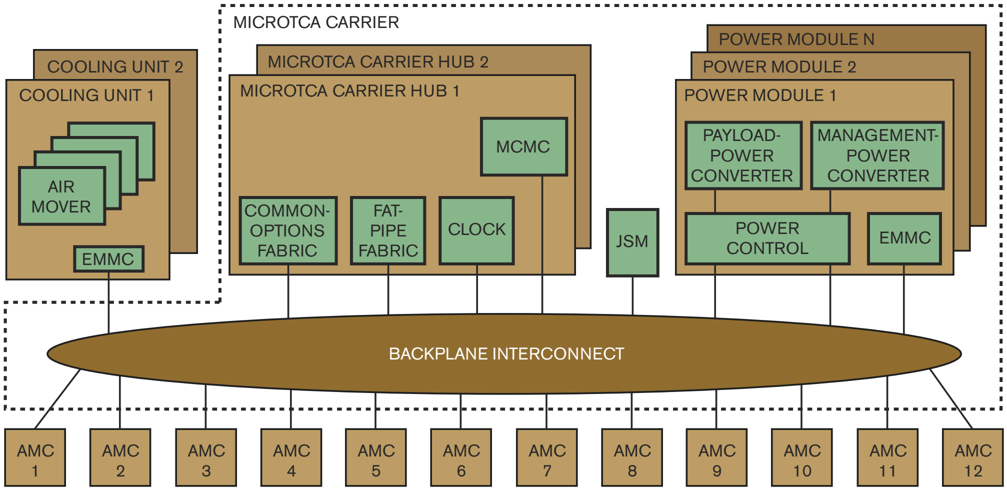

NOTES:
MCMC=MICROTCA CARRIER MANAGEMENT CONTROLLER.
EMMC=ENHANCED MODULE MANAGEMENT CONTROLLER.
JSM=JTAG SWITCH MODULE.

Figure 3 A typical MicroTCA system comprises as many as 12 AdvancedMCs, carrier hubs, power modules, a cooling subsystem, and a backplane interconnect.

fers designers a hot-swappable, field-replaceable module to lower maintenance costs and reduce downtime. AdvancedMC modules feature remote management and switched-fabric technology in an approximately 3×7-in. form factor. Modules come in single- or double-size configurations with compact, midsize, and full-size faceplates. AdvancedMC employs a subset of the same IPMI (Intelligent Platform Management Interface) that AdvancedTCA carrier cards require. This management-interface specification allows local and remote monitoring of equipment for power management, cooling, electronic keying, and hot-swap transactions.

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LT3477	SEPIC, Buck, Boost, Buck/Boost, Flyback, Inverter	100:1	2.5 to 36	2
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*Depends on external MOSFET

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LINEAR TECHNOLOGY

Artesyn Communication Products, recently announced an AdvancedMC module that it bases on the Intel Pentium M processor (**Figure 2**). The KosaiPM provides the localized horsepower necessary for applications such as protocol processing, packet processing, data management, and I/O management. The module features a low-power processor operating at as much as 1.8 GHz, 2 Mbytes of Level 2 cache, as much as 2 Gbytes of DDR SDRAM with ECC (error-correction code), a USB 2.0 interface, and a front-panel RS-232 console interface. To support high-speed packet-data transfers on and off the card, KosaiPM features both PCIe and dual Gigabit Ethernet interfaces to the baseboard. KosaiPM also features an I^2C-based IPMI that enables you to monitor the module and remotely control it. KosaiPM is also hot-swappable, reducing spares costs and mean time to repair.

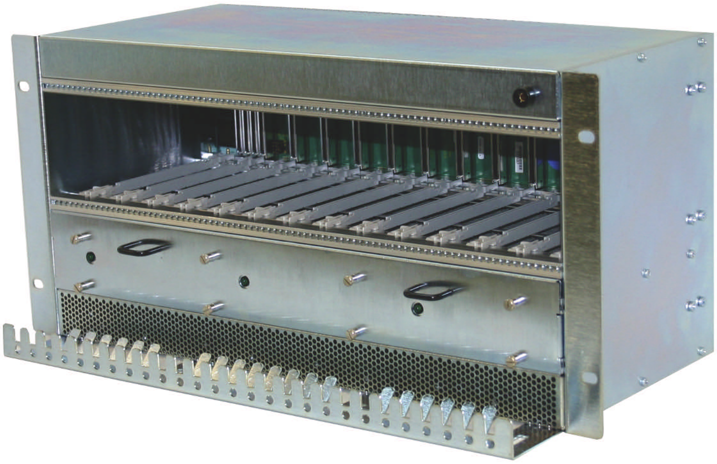
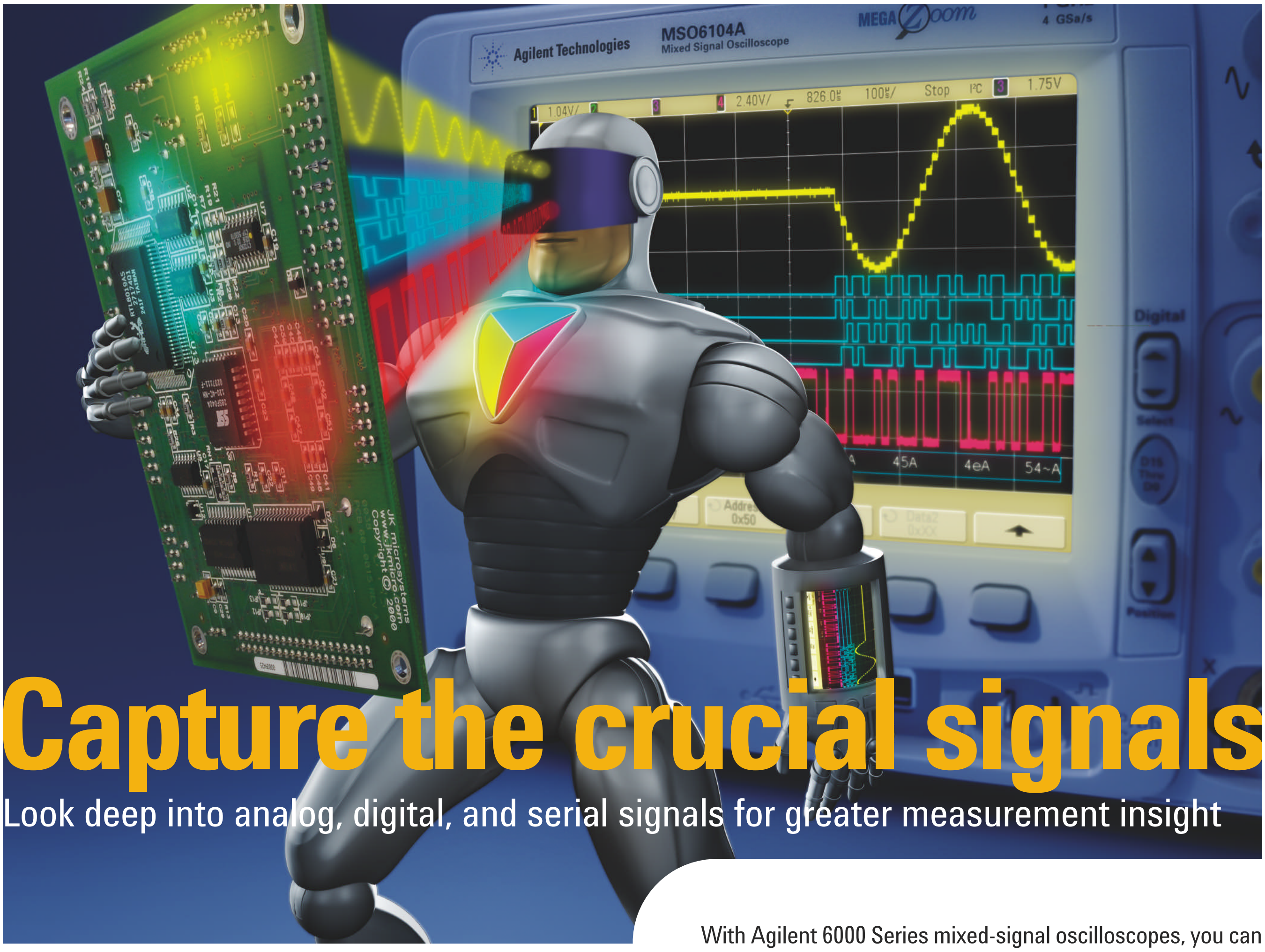


Figure 4 The new 5U MicroTCA shelf from Elma Electronic features a 14-slot dual-star backplane with 10 AdvancedMC, two power-module, and two carrier-hub slots.

With all the high-power, hot-swap, switched-fabric, and management features of AdvancedMC, designers considered using these modules to plug directly into a backplane for small, standalone systems. After considerable effort to get an industry consensus, PICMG released the MicroTCA specification in July 2006. MicroTCA provides a standalone chassis with a backplane that directly accepts AdvancedMC cards, thereby eliminating the AdvancedTCA carrier board. The smaller form factor makes the concept viable for lower budget applications in telecom and a range of embedded-system projects.

The short-form version of the MicroTCA specification, available at the PICMG Web site, defines a minimum MicroTCA system as a collection of interconnected elements consisting of at least one AdvancedMC module; at least one MicroTCA carrier hub; a power module; and the interconnect, cooling, and mechanical resources needed to support them. A MicroTCA carrier hub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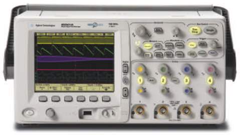

combines the control and management infrastructure and the interconnect-fabric resources necessary to support as many as 12 AdvancedMCs in a single module. The MicroTCA power module takes the input supply and converts it to 12V to provide payload power to each AdvancedMC module. As an example, a typical MicroTCA system comprises as many as 12 AdvancedMCs, one or two carrier hubs, multiple power modules, load sharing, a cooling subsystem, a backplane interconnect, and the mechanical elements (**Figure 3**). You can duplicate active components to provide redundancy. Elma Electronic recently announced a new 5U MicroTCA shelf with a 14-slot dual-star backplane in the single-module, full-size format. The backplane provides 10 AdvancedMC, two power-module, and two MicroTCA carrier-hub slots (**Figure 4**). Three plug-in fan trays with air filtering provide cooling. Prices for the 5U MicroTCA shelf starts at less than $2000, depending on options.

Whether a standard evolves from a previous version or starts from scratch, the developers are searching for the same thing: a stable open specification that allows diverse manufacturers to produce technologically advanced boards that work together for the lowest possible price. An ample supply of readily available COTS boards is vital to the high-performance, embedded-system-development process. As embedded-system developers concede, there is no Holy Grail of open standards that applies to every project, and there probably never will be. Instead, as electronics technology continues to conform to Moore's Law, you will see a steady stream of standards updates plus plenty of completely new ideas (see **sidebar** "Stackables seek a new direction"). The alternative is to return to the long lead times and hefty budgets of in-house, proprietary designs.**EDN**

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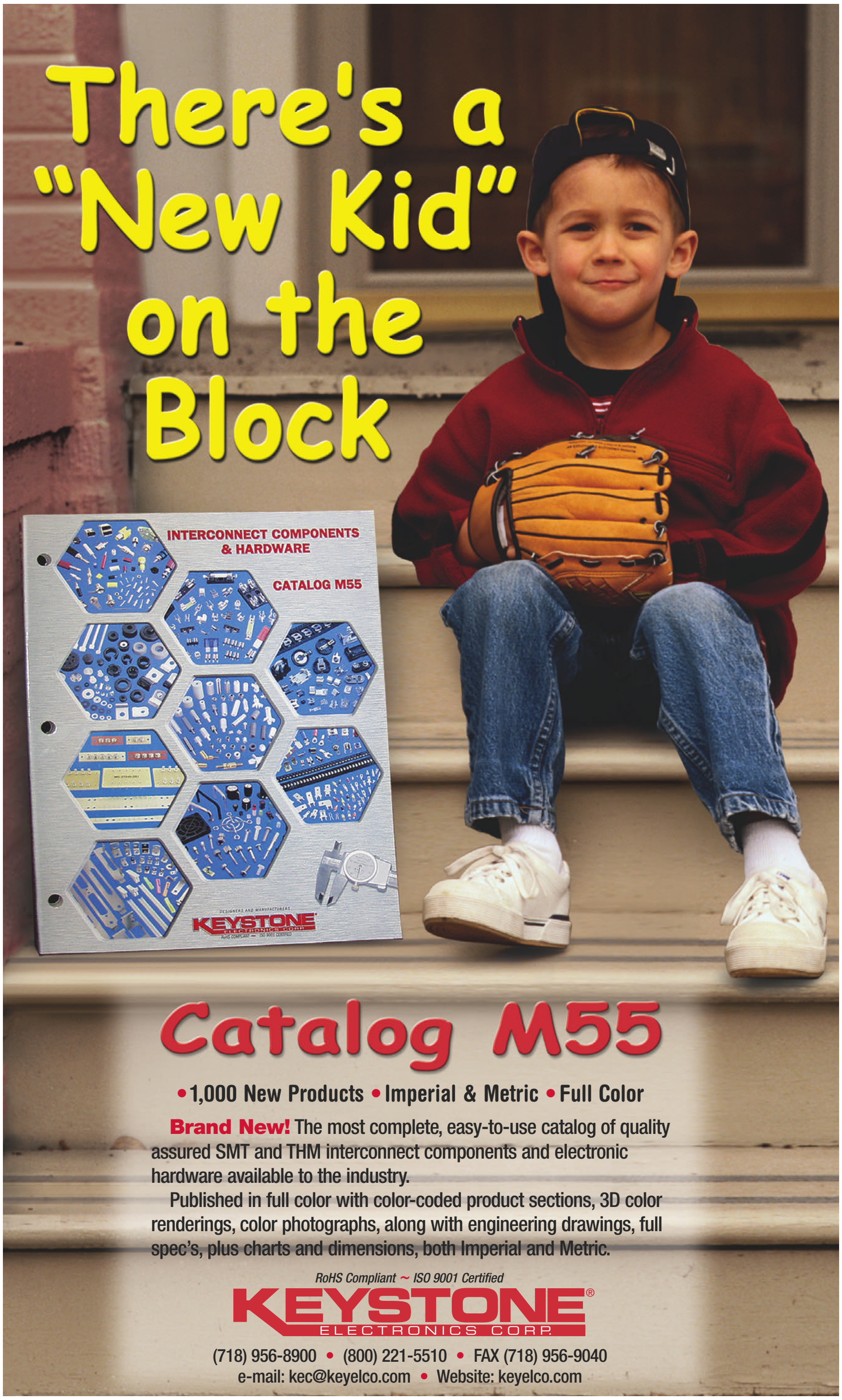

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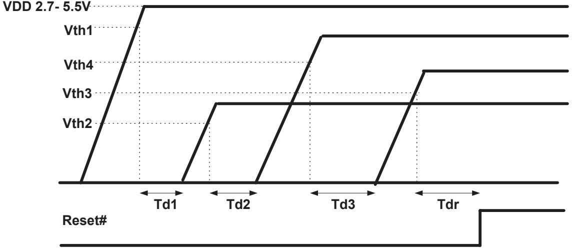

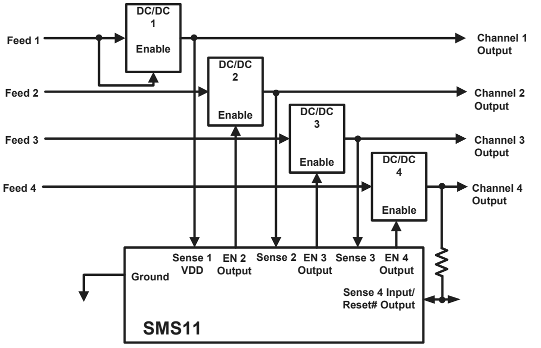

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Sequencing Order/Delay	Prog	Capacitor	Capacitor	Prog
Reset Timeout	Prog	Capacitor	Capacitor	Prog
# External components	0	13	17	5
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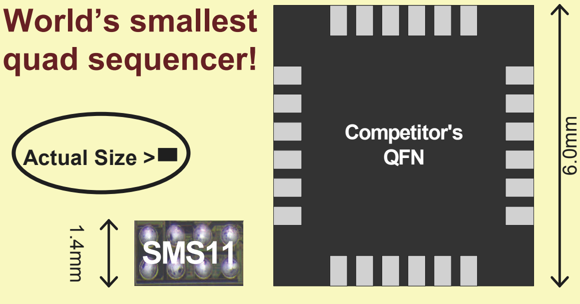

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Voltage Monitor Threshold	Prog	N/A	Fixed	Fixed/Resistor
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Package Type	CSP-6	DFN-8	SOT-23	SOT-23
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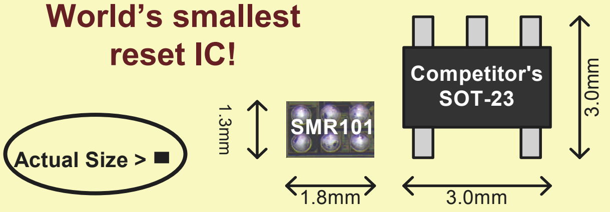

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Choosing to use an SIP

DEVELOPING AN SIP PRODUCT RATHER THAN AN SOC FOR A PORTABLE MULTIMEDIA PLATFORM BEGINS WITH CAREFUL ARCHITECTURE PLANNING.

This development of austriamicrosystems' second-generation multimedia platform and its derivative products exemplifies the advantages that an SIP (system-in-package) product can offer over an SOC (system on chip). The design team created performance-critical IP (intellectual-property) blocks and used IP blocks from outside vendors to speed the development and to reduce the costs of such a complex undertaking. The team carefully chose the criteria for selecting and purchasing IP and encountered several problems with the integration of some IP blocks. Many CAD tools contributed to the development, but there are still development tasks, especially in the area of hardware/software co-design and in the design of the SIP, that commercially available tools cannot handle. Close cooperation between the hardware team and the software team was necessary to obtain optimal performance from the products. In addition, the team considered design-for-test and design-for-manufacturability issues early in the development cycle.

DESIGN REQUIREMENTS

Product development starts with the requirement inputs from sales and marketing and with an in-depth analysis of competitive products. This product targets portable players and handles all available audio formats, including the latest DRM (digital-rights-management) and audio enhancements, such as bass boost, equalizer, and others. To be as flexible as possible, it interfaces to flash-storage media and to hard disks. High Speed USB 2.0 guarantees high-speed music downloading from PCs, and the USB OTG (On-The-Go) function enables high-speed file exchange between players without a PC. Most low-cost portable audio players offer at best low-performance audio recording, and AA or AAA batteries power them; high-performance players have color LCDs, offer CD-quality recording, and use lithium-ion batteries, including a charger that works from either an external dc supply or from the USB (**Figure 1**).

The feasibility analysis demonstrated that an SOC could not handle all requirements and that the design required at least two products—a high-end product with all features and a low-cost product. A key performance differentiator for both products is power consumption, which you measure as the play time with an AA battery during MP3 playback with headphones. To achieve the lowest power consumption, the design team chose an ARM9 hard-wired core with on-chip RAM, which the team judged big enough for the applications: high-efficiency dc/dc converters and a low-power DAC and headphone amplifier. In addition, the team's efforts to minimize total cost influenced the choices for chip size; assembly costs; and level of integration, including the number and cost of external components, production-test time, and total yield.

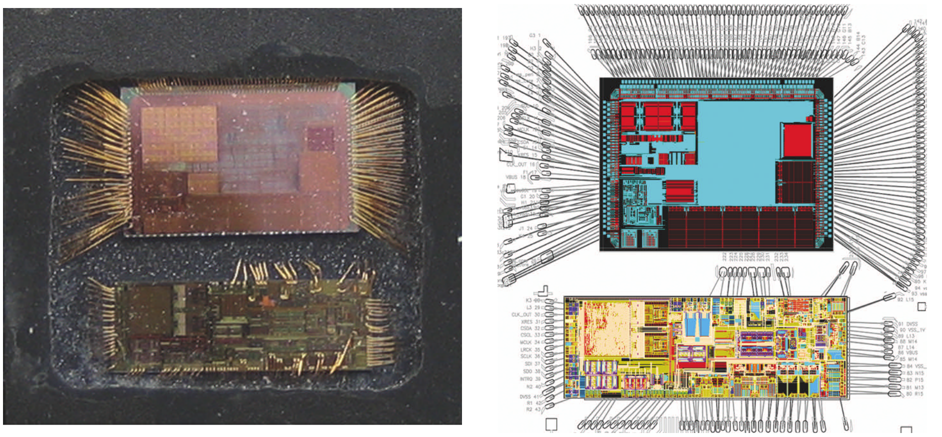

Figure 1 Separate analog (left) and digital (right) die constitute this SIP.

To this end, the team compared SOC and SIP approaches. The advantage of an SOC implementation is cheaper logistics, because using an SOC means that you are handling only a single die during wafer sorting and assembly. In addition, the chip package is simpler, the assembly costs are lower, and the risk of cross-coupling inside the package is smaller. An SIP requires careful partitioning to avoid large chip-area overhead and power loss in the interface between the die. On the other hand, it holds significant advantages: Digital processing is possible in the smallest available process technology, whereas the product can complete analog-processing and power-management functions in a robust technology that can handle as much as 5.5V and, perhaps, 15V for the white-LED-backlight driver. Despite the difficulties of handling two wafers and the complex two-die assembly, the use of an SIP resulted in the lowest chip costs (**Figure 2**). Note that this comparison includes all expenses from wafer costs, wafer sort, SIP assembly, and final test. SIP also let the designers quickly launch an entire product family with a platform and several derivative products.

The team started the project at the end of 2003 and decided to use 130-nm-CMOS technology for the digital processor. The reasons for this decision included feature requirements and product positioning; the availability of IP blocks, especially the processor core and the high-density on-chip RAM; and the robustness of the technology at the time-of-production ramp, which the team planned for early 2005. The process technology's robustness was an assumption at the project's start for which the team had to complete a risk assessment. The designers implemented the analog-audio and power-management functions in a 3.3/5V, 0.35-micron CMOS-process technology with PIP (polysilicon-insulator-polysilicon) capacitors. Austriamicrosystems has a large portfolio of silicon-proven and highly optimized IP blocks available in this process and could investigate several performance improvements and area optimizations when making two die—one for the low-cost products and one for the high-end market. Combining the digital die with analog die and a 16-Mbyte SDRAM die, the designers developed five products (**Figure 3**).

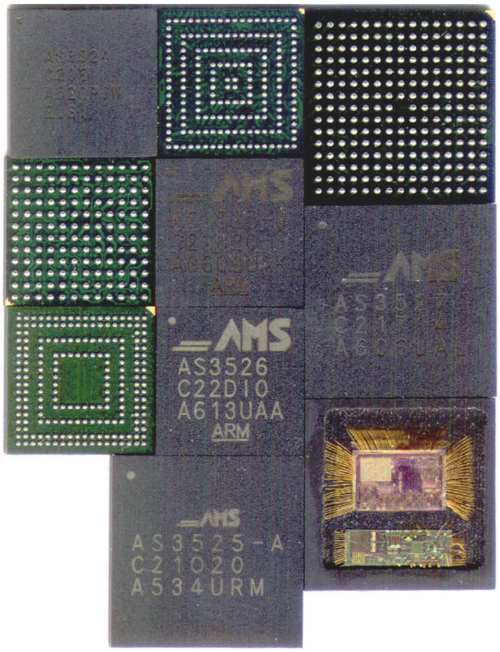

Figure 2 You can combine the SIP with memory chips in a number of configurations.

A team of marketers, product managers, digital- and analog-hardware designers, and software developers completed the system definition. Using the knowledge from the first-generation products, they developed many important design improvements. The team analyzed cases and accordingly optimized the architecture using tools such as Mentor Graphics (www.mentor.com) Seamless and relying heavily on FPGA prototyping. Because EDA-tool support was poor, however, the designers used spreadsheets for many calculations.

THE JOYS OF IP

Any consumer product requires a short development, which you can theoretically achieve using in-house and purchased IP blocks. The team therefore tried to adhere to the following strategy: Search for process-proven IP, check for performance and qualification, and negotiate price and legal conditions. If the IP were available from different vendors, the team would make a detailed comparison; if it were not yet process-proven, the team would work out a common development schedule; if the IP were not technically or commercially available, the team would develop its own.

Not all purchased IP blocks were complete at the project's start, creating a major risk issue in product development. At the project's start, the designers agreed on a fixed schedule with IP providers, but they had four major problems:

- The development schedule slipped at an IP provider. The team had many incremental changes during the tapeout phase and had to implement several last-minute ECOs (engineering-change orders). As a result, the team had to twice perform the physical design, which delayed the schedule and significantly increased the development costs.
- One IP block that the designers had considered as a fully qualified block didn't work over the full temperature range and required metal redesigns.
- The performance of one IP block was not fully in spec with typical wafer material and required another metal-mask redesign, which the team did after analyzing the performance on a wafer-split lot.
- One IP block didn't work according to the specifications, and the supplier couldn't fix the problems. The team got involved in depth in the design and substantially modified it. This approach was possible only because the team knew how to complete such a complex task.

In fact, for this project, the team developed several IP blocks, mainly to have a competitive advantage for all performance-critical blocks. These blocks include the NAND-flash interface, for which the designers had built system knowledge; the chip-control and clock-generation units, which aim to optimize the system-power consumption; the flexible display interface, which targets use in small displays with internal microcontrollers; all power-management blocks, including dc/dc converters, charge pumps, low-dropout regulators, and chargers; and the analog-audio blocks.

THE DESIGN FLOW

The designers used a state-of-the-art digital-design flow. The front-end flow comprised careful floorplanning; hierarchical-module synthesis, including scan-test-ready compilation; gray-box modeling for top-level timing; module-level RTL verification; and top-level verification using integration-test registers. Flat timing-driven place-and-route flow ran as follows: place, clock-tree insertion, scan stitching, route, and hold fixing. Analysis steps included static-timing analysis, RC-corner extraction, logic-equivalence checking, IR drop, electromigration checking, crosstalk analysis, cell-level LVS (layout-versus-schematic) analysis, transistor-level LVS analysis of the I/O-pad ring, and final design-rule checks and design-for-manufacturing routines.

The first tapeout was on a multiproject wafer run to reduce the costs and risk. A minor feature was missing, but the designers wanted to keep the shuttle date and sent the GDSII (Graphic Design System II) file for manufacturing. The first silicon was fully functional and worked in spec, and the designers started software development with these samples. Then, they had to add a "minor" missing feature that they couldn't implement in a simple ECO that required a full synthesis and complete physical design. Finally, marketing requested S/PDIF (Sony/Philips Digital Interface Format), which the team implemented on a redesign of the analog die for only the high-end version.

The team achieved best-in-class power consumption for the product using a hard-wired ARM922T core; 320 kbytes of on-chip RAM; three dc/dc step-down converters for core, hard-

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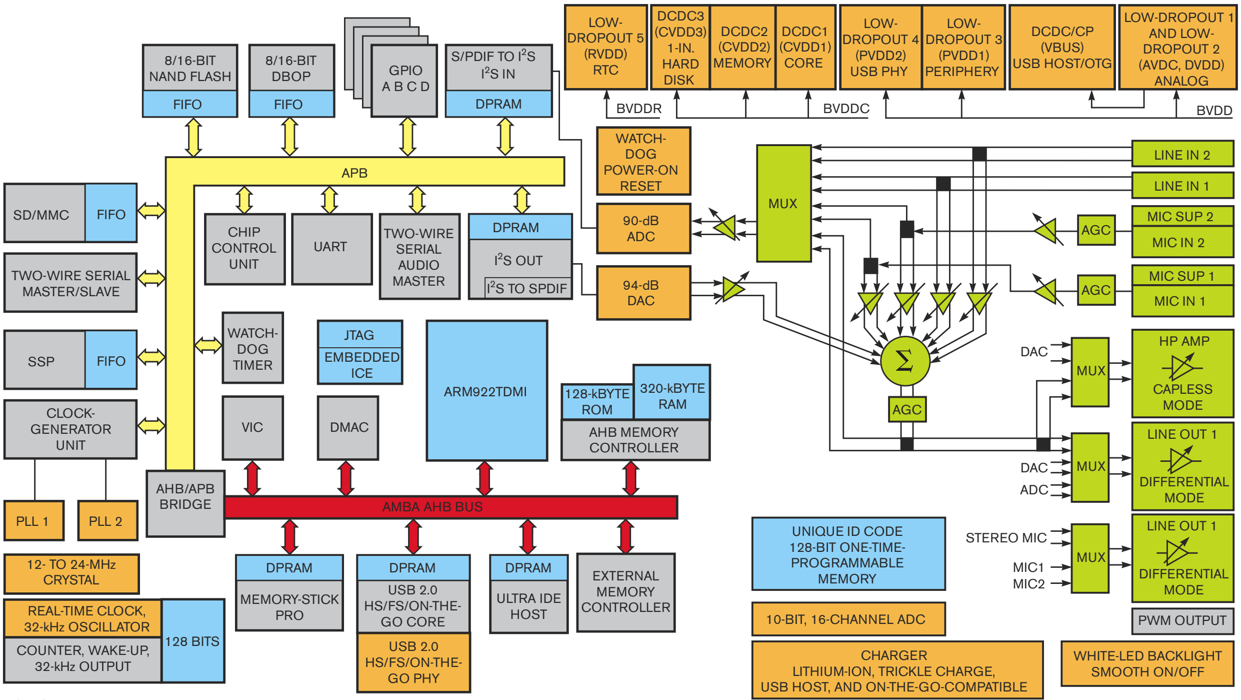

NOTES:
MUX=MULTIPLEXER.
GPIO=GENERAL-PURPOSE INPUT/OUTPUT.
DMAC=DIRECT-MEMORY-ACCESS CONTROLLER.
MIC=MICROPHONE.
DBOP=DATA-BLOCK OUTPUT PORT (DISPLAY INTERFACE).
DPRAM=DUAL-PORT RAM.
RVDD=REAL-TIME-CLOCK SUPPLY VOLTAGE.
CVDD=HARD-DISK, MEMORY, AND CORE SUPPLY VOLTAGES.
PVDD=PERIPHERY SUPPLY VOLTAGES.
VBUS=USB 5V SUPPLY.
SD/MCC=SECURE-DIGITAL/MULTIMEDIA CARD.
APB=ADVANCED MICROCONTROLLER BUS ARCHITECTURE (AMBA) PERIPHERAL BUS.
AHB=AMBA HIGH-SPEED BUS.
VIC=VECTORED-INTERRUPT CONTROLLER.
HS=HIGH SPEED.
FS=FULL SPEED.
S/PDIF=SONY/PHILIPS DIGITAL INTERFACE FORMAT.
DVDD=DIGITAL-PART SUPPLY VOLTAGE.
AVDD=ANALOG-PART SUPPLY VOLTAGE.

Figure 3 The AS3527 SIP is a full, high-performance portable-audio player.

disk, and memory supply; a high-performance, Class AB, low-power headphone amplifier; and a low-power, high-performance, 18-bit sigma-delta DAC. The designers developed high-level VHDL-AMS (very-high-speed-IC hardware-description-language-analog-mixed-signal)-simulation models to optimize the system-power consumption and simulated the play time with AA and lithium-ion batteries. Another challenge was the combination of audio and power management, especially noisy dc/dc converters, in a single package. The die and the BGA substrate achieve better than 93-dB SNR.

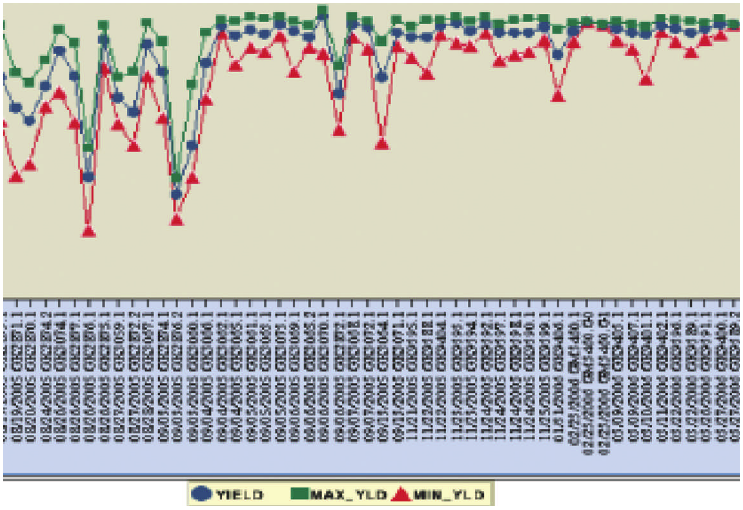

Figure 4 Continuous effort has brought SIP yield up to typical SOC levels.

The team developed tools to handle two- and four-layer BGA substrates. The motivations were the long substrate-manufacturing times and the errors with BGAs, which had occurred with previous designs. Finally, the team achieved correct connectivity, crosstalk-analysis investigations, and the verification of current densities and series resistances.

The team designed boards for chip evaluation and software development that use a common motherboard with a color display, keys, storage media, and dedicated daughterboards for each product with all components for IC operation, including capacitors, coils, ESD protection, and USB connectors.

Production can start only with fully qualified hardware and software, and the team tried to start the software development as early as possible. To enable hardware/software co-design, the designers used FPGA prototyping and a hardware/software-co-design tool. Unfortunately, the FPGA implementation differed from the IC implementation due to many restrictions in the FPGA design. Al-

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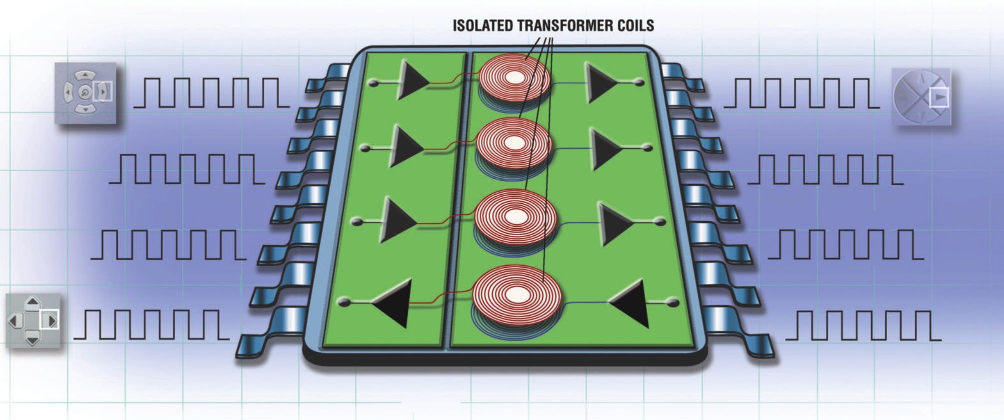

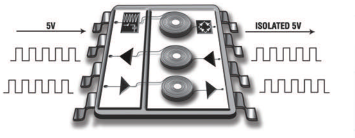

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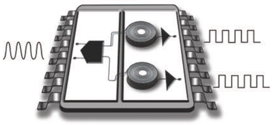

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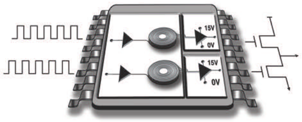

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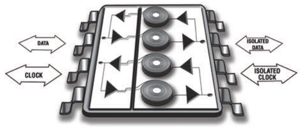

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ANALOG DEVICES

so, the designers had only a few models available on the hardware/software co-design tool, and simulation speed was low. As a result, the real software-design work effectively started only when samples first became available in silicon, and the team needed another mask for the ROM update to make the final boot loader. It then took some time until the designers could demonstrate a flash player for WMA (Windows Media Audio), DRM, and MTP (Media Transfer Protocol), which works without external SDRAM and conforms to PlaysForSure. The team achieved this goal by using a lean operating system, optimized device drivers for the NAND flash and USB, optimized WMA and DRM code, and a reloader concept with application swapping.

Production testing of SIPs requires high test coverage at wafer sort to minimize product costs. At wafer sort, the designers used full test of the digital die using BIST (built-in self-test), ATPG (automatic-test-pattern-generation)-scan test, and at-speed functional testing to detect process variations as early as possible. They undertook full testing of the analog die using analog-test multiplexers and highly speed-optimized test procedures and succeeded in developing a package that can perform more than 600 analog tests in a short time.

To produce this SIP, the team needed fully functional samples, including a software-development board and a software-development kit, which provides not only all hardware drivers, but also a reference player for performing the certification tests for, for example, USB and PlaysForSure. The wafer-sort test programs for each die must have high test coverage to avoid costly yield loss at final test of the BGA package. Finally, a product qualification is necessary to guarantee highest quality. During production ramp-up, the team carefully monitored the production yield at wafer sort and at final test and optimized the yield for the product during the first wafer lots (**Figure 4**). All this work has paid off. Today, yield for the SIP is similar to that of an equivalent-sized SOC product.

Despite the numerous problems during the design phase of this SIP portable-audio-player product, austriamicrosystems was able to solve all issues with several IP providers and successfully combined a 130-nm-CMOS die with digital interfaces and processing and a 0.35-micron-CMOS die with high-efficiency power management and high-performance audio in a single BGA package.**EDN**

AUTHOR'S BIOGRAPHY

Mario Manninger is director of engineering in the communications business unit austriamicrosystems, where he has worked for more than 15 years and is responsible for analog/mixed-signal-IC design and SOC development. He has a master's degree in electrical engineering from the Technical University of Graz (Austria) and enjoys skiing, wind-surfing, tennis, catamaran-sailing, and visiting foreign countries.

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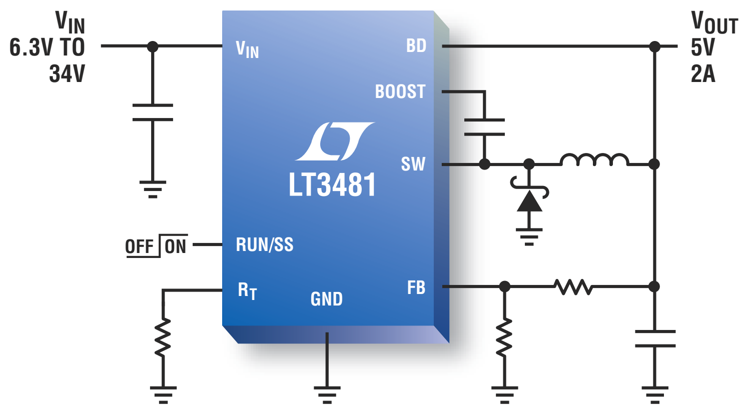

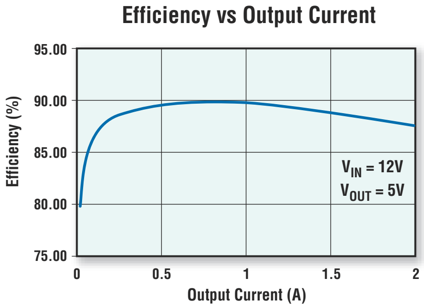

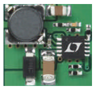

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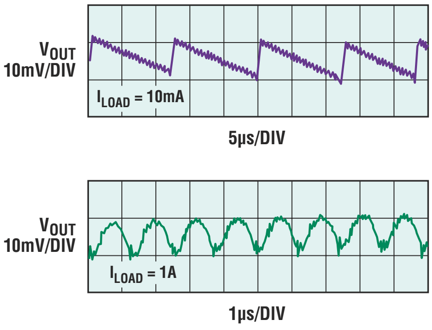

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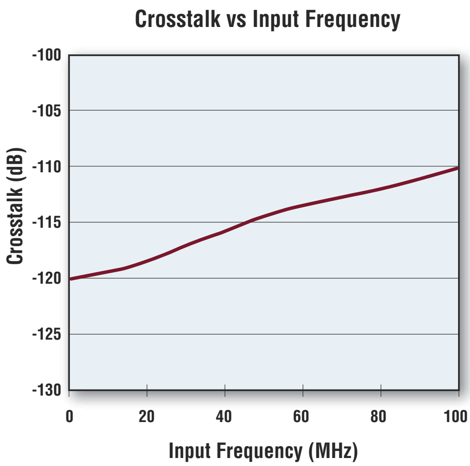

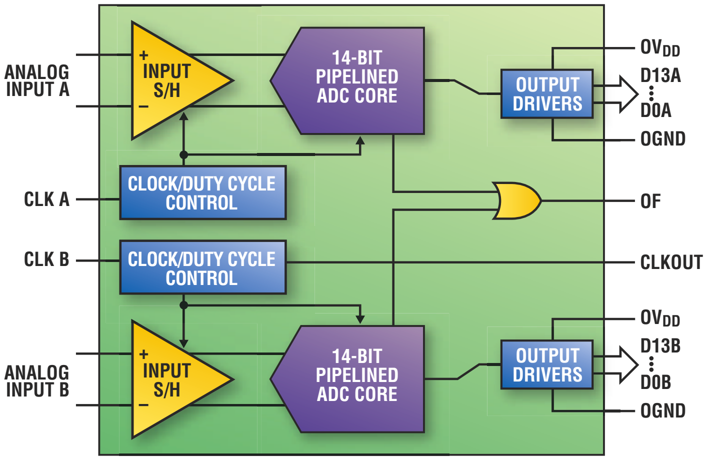

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LINEAR TECHNOLOGY

EDITED BY BRAD THOMPSON
AND CHARLES H SMALL

Linear-brightness controller for LEDs has 64 taps

Ahmad Ayar, Maxim Integrated Products, Sunnyvale, CA

Applications that include LEDs but no microcontroller or other form of control intelligence can benefit from a simple circuit that provides manual control of the LEDs' light intensity. Among the devices suitable for this purpose are mechanical (analog) and electronic (digital) potentiometers. The digital potentiometer with up and down pushbuttons, an alternative to the mechanical potentiometer, is smaller, more reliable, and usually less expensive (**Figure 1**).

IC_2, a current regulator, drives a chain of LEDs with current as high as 200 mA. In a standard application circuit, IC_2's internal regulator senses the drop across current-sense resistor R_{SENSE} in series with the LED chain. Thus, IC_2 controls current through the chain by regulating voltage at the differential inputs, CS− and CS+, to the set value of 204 mV. Resistors R_A and R_B allow the output voltage IC_1's Pin 6 to adjust the current level. IC_1 is a 64-tap linear digital potentiometer whose resistance connects between ground and V5, a well-regulated voltage that IC_2 internally generates. You manually adjust the RW control voltage (Pin 6), a fraction of V5, using the up and down pushbuttons. A few assumptions allow a quick and simplified calculation of the necessary resistor values. Initially, you fix R_A and then calculate R_B and R_{SENSE}. The assumptions are that you can neglect the maximum 6.93-μA error induced by the bias current at CS+; that the value you choose for R_A is much higher than IC_1's equivalent resistance, for which the worst-case value at position 32 (top and bottom resistances plus the wiper series resistance) is 2.9 kΩ; and that R_{SENSE} is much less than R_B.

After setting R_A at 25.5 kΩ, $V_{WIPER}=(5V/63)\times N$, where N is the wiper setting (0 to 63). Then, you solve the equation $(V_{WIPER}-0.204V)/R_A=(0.204V-I_{LED}\times R_{SENSE})/R_B$. Solve the above equation for R_B under the conditions for which $I_{LED}=0$, which are $N=63$ and $V_{WIPER}=5V$ (top position): $R_B=25.5\ k\Omega\times 0.204V/(5V\times 0.204V)=1.085\ k\Omega$. You can choose R_B from the standard values of 1.07 kΩ (1% series) or 1.1 kΩ (5% series). At the bottom position, where $V_{WIPER}=0$ and LED current is the maximum of 200 mA, brightness should be the maximum available. Solving for R_{SENSE}, $R_{SENSE}=[0.204V+(0.204V\times(1.085/25.5))]/0.2A=1.063\Omega$; 1.07Ω is a standard value in the 1% series.

A graph of LED current versus tap position shows a slight nonlinearity

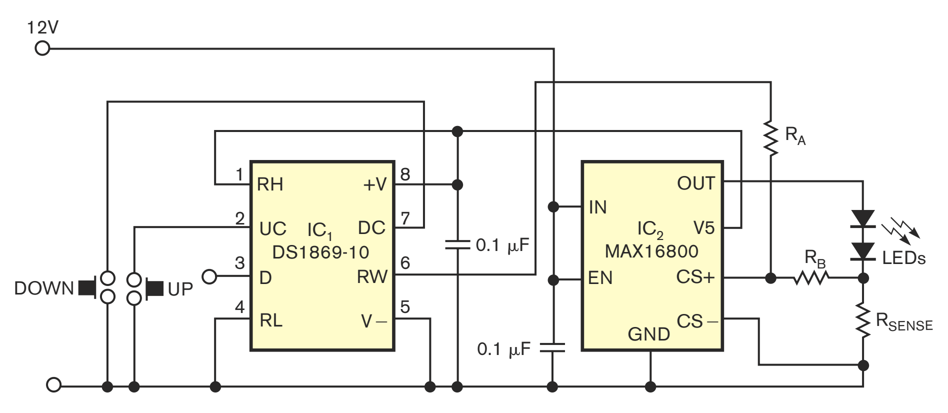

Figure 1 This brightness-control circuit lets you manually adjust the LED brightness using the up and down buttons.

DIs Inside

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because of the variation in resistance you see looking into the wiper at different tap positions (**Figure 2**). At the extreme ends of the potentiometer, you see only the 400Ω wiper resistance. As the wiper moves toward midpoint, the resistance increases toward a maximum of one-quarter of the end-to-end resistance value. Because IC_1 is a 10-kΩ potentiometer, the resistance the wiper sees at midpoint is about 2.5 kΩ in series with R_{WIPER}. This variation introduces a maximum linearity error of 8%, which is negligible in most LED applications. IC_2 offers thermal protection against excessive heat and overload conditions. For effective power dissipation and to avoid thermal cycling, you must connect the exposed pad of the package to a large-area ground plane.**EDN**

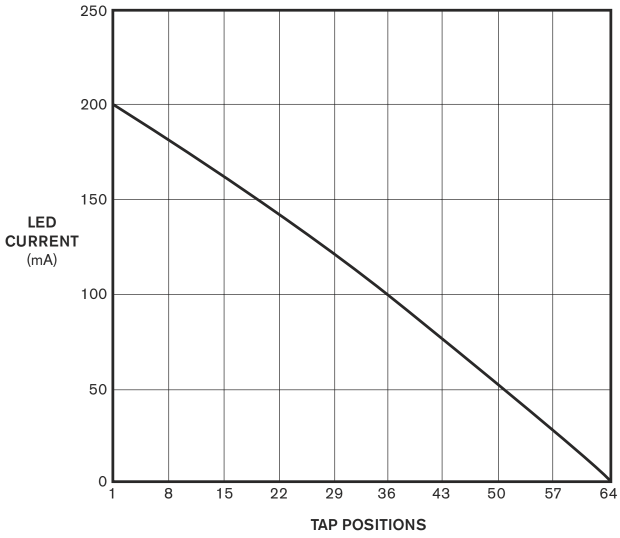


Figure 2 A plot of LED current versus tap position in Figure 1 exhibits only a slight nonlinearity.

Controlled power supply increases op amps' output-voltage range

Yakov Velikson, Lexington, MA

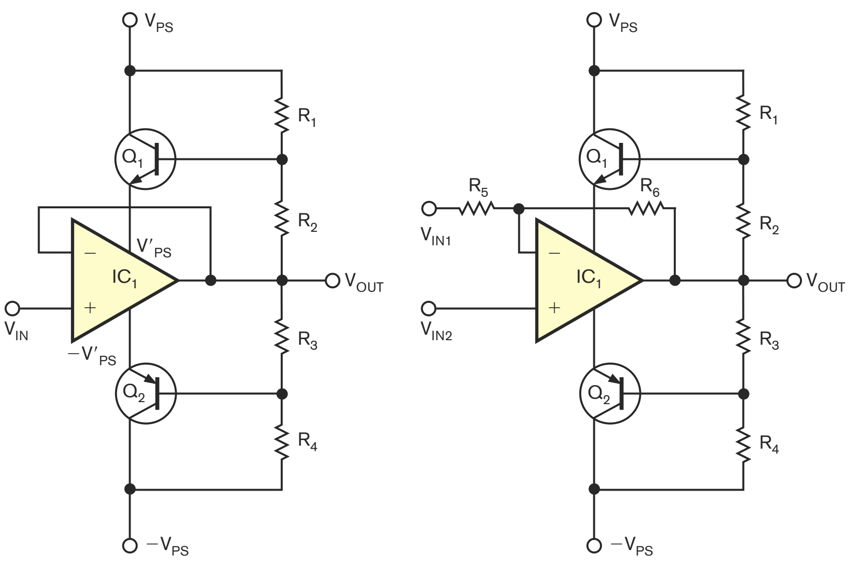


Figure 1 These simple circuits present the general methods of connecting the amplifier as an inverter or a follower to effect increased output voltage.

Increasing the output voltage of IC operational amplifiers usually involves adding high-voltage external transistors. The resulting circuit then requires correction to retain its operating characteristics. This correction is difficult, especially for precise amplifiers. This Design Idea presents an alternative: the use of a controlled power supply for the operational amplifier itself, which can increase the output voltage for many precise operational amplifiers without altering their operational characteristics. You can accomplish this task by connecting controlled transistors to the power supply of the amplifier. Resistor dividers that connect to the amplifier's output and bipolar high voltages control these transistors (**Reference 1**). The simple circuits in **Figure 1** present general methods of connecting the amplifier as an inverter or a follower to effect increased output voltage.

Dividers with resistors R_1, R_2, R_3, and R_4 determine the scale of power supply V'_{PS} and $-V'_{PS}$ for the amplifiers. If the output voltage ranges from ±22V,

Any V_{IN} to Any V_{OUT}

V_{IN} & V_{OUT}

36V

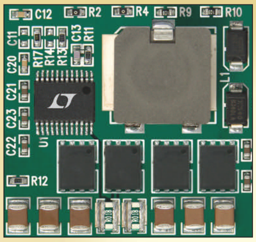
0.8V

I_{OUT}

12A

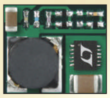
0A

60W



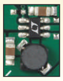
LTC3780

5W



LTC3443

1W



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LTC3440	2.5 to 5.5	2.5 to 5.5	0.6	300kHz to 2MHz	25	3x3 DFN, MSOP-10
LTC3530	1.8 to 5.5	1.8 to 5.25	0.6	300kHz to 2MHz	40	3x3 DFN, MSOP-10
LTC3441	2.4 to 5.5	2.4 to 5.25	1.2	1MHz	25	3x4 DFN
LTC3442	2.4 to 5.5	2.4 to 5.25	1.2	300kHz to 2MHz	35	3x4 DFN
LTC3443	2.4 to 5.5	2.4 to 5.25	1.2	600kHz	28	3x4 DFN
LTC3785*	2.7 to 10	2.7 to 10	10.0†	100kHz to 1MHz	80	4x4 QFN, SSOP-28
LTC3780	4 to 36	0.8 to 30	12.0†	200kHz to 400kHz	1.5mA	5x5 QFN, SSOP-24

† Depends on MOSFET selection, *Future Product

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resistor $R_1=R_2=R_3=R_4=R$, and V_{PS} and $-V_{PS}$ are 28V, then voltages V'_{PS} and $-V'_{PS}$ fall in the following range, allowing for any additional loss: $V'_{PS}=V_{PS}R_2/(R_1+R_2)+V_{OUT}(-V_{OUT})R_1/(R_1+R_2)$, and $-V'_{PS}=-V_{PS}R_3/(R_3+R_4)+V_{OUT}(-V_{OUT})R_4/(R_3+R_4)$ or $3V<V'_{PS}<25V$ and $-3V>-V'_{PS}>-25V$. However, power-supply circuits include transistors, which create junction resistance, affecting the amplifier's operation.

You can use supporting amplifiers to reduce losses and increase the quality of the output voltage of the primary amplifier. The requirements for supporting amplifiers are simple. They should have power supplies with opposite polarity from and lower applied voltage than that of the main power supply. They should provide the necessary power to the primary amplifier, and their frequency range should be slightly higher than that of the primary amplifier. You can use supporting amplifiers to eliminate the transitional resistances of transistors in power-supply connections. Thus, these circuits offer flexibility across a range of amplifier configurations (**references** 2 and 3).

Figure 2 shows an example of how to connect supporting amplifiers as followers. You derive output voltages V'_{PS} and $-V'_{PS}$ from resistor connections with the following equations: $V'=V_{PS1}R_7/(R_6+R_7)+V_{OUT}(-V_{OUT})R_6/(R_6+R_7)$, and $-V'=-V_{PS1}R_8/(R_8+R_9)+V_{OUT}(-V_{OUT})R_9/(R_8+R_9)$. If the supporting amplifiers have a power supply of 28V for V_{PS1} and $-2V$ for $-V_{PS2}$ for amplifier IC_2, then $-V_{PS1}=-28V$, $V_{PS2}=2V$ for amplifier IC_3, and the output voltage of amplifier IC_1, V_{OUT}, is 24V or $-24V$. Also, $R_6=R_7=R_8=R_9=R$, such that $V'=28V\times0.5+24V\times0.5=26V$. Further, $-V'=-28V\times0.5+24V\times0.5=-2V$ for $V_{OUTMAX}=24V$. $V=28V\times0.5-24V\times0.5=2V$, and $-V'=-28V\times0.5-24V\times0.5=-26V$ for $V_{OUTMIN}=-24V$. You can achieve the greatest voltage range by using separate power supplies—one for the normal voltages of the amplifier and one for the regulated part of the output voltage (**Figure** 3).

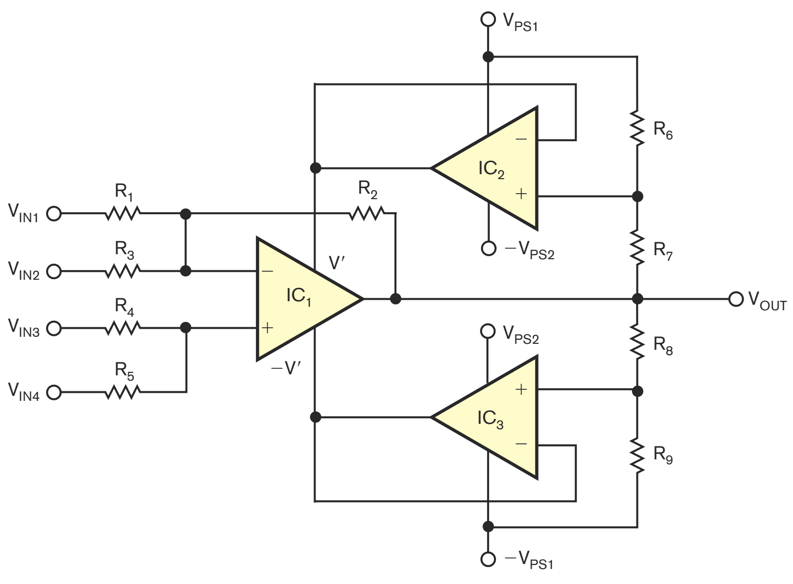

Figure 2 Replacing the transistors with op amps reduces losses and increases the quality of the output voltage of the primary amplifier.

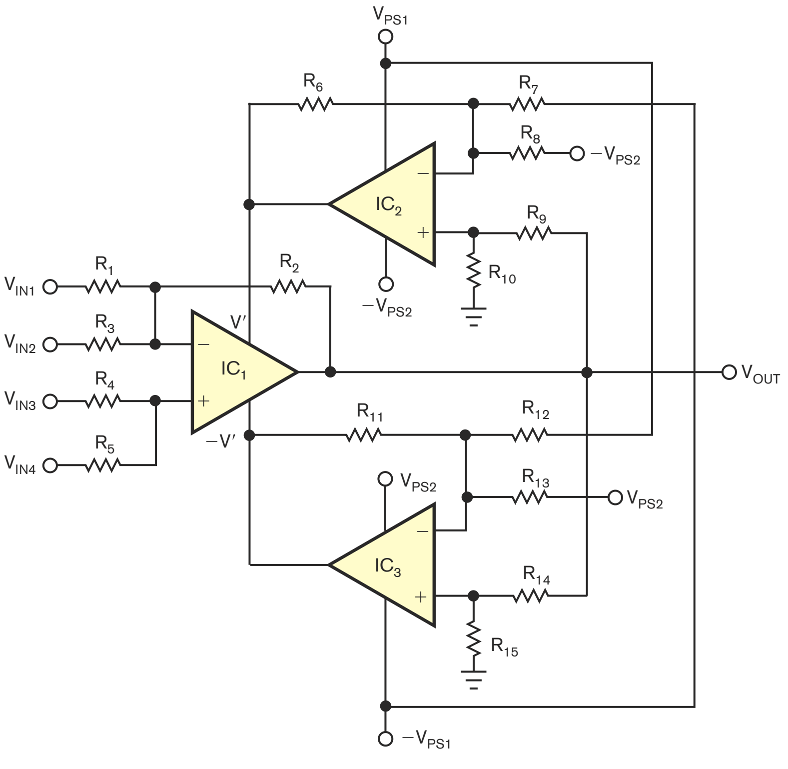

Figure 3 You can achieve the greatest voltage range by using separate power supplies—one for the normal voltages of the amplifier and one for the regulated part of the output voltage.

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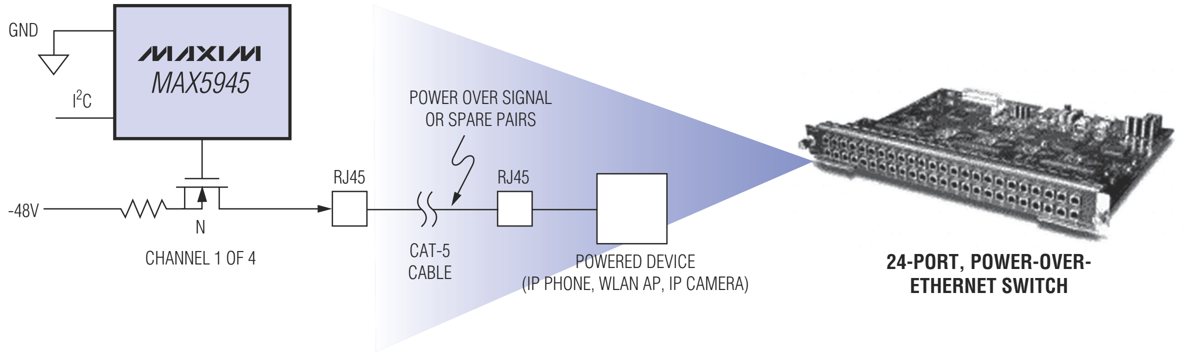

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IC_1 is the primary amplifier. Supporting amplifiers IC_2 and IC_3 have asymmetrical power supplies. You could use many types of amplifiers in this circuit, but modern operational amplifiers may be preferable because they allow the use of the complete range of the power supply and because they handle rail-to-rail input and output. In this circuit, $V_{PS1}=28V$, $-V_{PS1}=-28V$, $V_{PS2}=2V$, and $-V_{PS2}=-2V$. The voltages of the primary amplifier are $V'=-(-V_{PS1})R_6/R_7-(-V_{PS2})R_6/R_8+(-V_{OUT})R_{10}/(R_9+R_{10})[R_7R_8+R_6(R_7+R_8)]/R_7R_8$. Further, $-V'=-(V_{PS1})R_{11}/R_{12}-(V_{PS2})R_{11}/R_{13}+(-V_{OUT})R_{15}/(R_{14}+R_{15})[R_{12}R_{13}+R_{11}(R_{12}+R_{13})]/R_{12}R_{13}$. Set $R_6=R_{10}=R_{11}=R_{15}=R$, $R_7=R_8=R_{12}=R_{13}=2R$, and $R_9=R_{14}=3R$, such that $R_6/R_7=R_6/R_8=R_{11}/R_{12}=R_{11}/R_{13}=0.5$, $R_{10}/(R_9+R_{10})=R_{15}/(R_{14}+R_{15})=0.25$, and $[R_7R_8+R_6(R_7+R_8)]/R_7R_8=[R_{12}R_{13}+R_{11}(R_{12}+R_{13})]/R_{12}R_{13}=2$. Then, substitute these values into the amplifier voltages yields $V'=14V+1V+(-V_{OUT})0.5$, and $-V'=-14V-1V+(-V_{OUT})0.5$. Minimum and maximum values for each power supply are $1.5V \le V \le 28.5V$, and $-1.5V \ge -V \ge -28.5V$. The total voltage of the power supply has a limit of 30V, ranging from 1.5 to 28.5V and from −1.5 to −28.5V. This range permits an increase of the output voltage of the primary amplifier by ±27V. **EDN**

REFERENCES

1. Velikson, Yakov, *Electronics, Information Book*, pg 138, Energoatomiztum, St Petersburg, Russia, 1996.
2. Velikson, Yakov, "Device for recurrence of voltage," *Bulletin of Izobreteny* (copyrights and patents), No. 3, 1991.
3. Velikson, Yakov, A Murigin, and V Uchno, "The multichannel conversion of a revolving sine-cosine resolver to code," *Bulletin of Izobreteny* (copyrights and patents), No. 44, 1988.

Single-IC-based electronic circuit replaces mechanical switch

Santosh Bhandarkar, Bangalore, India

A simple and inexpensive electronic circuit uses a low-cost pushbutton switch to toggle the electrical power on and off. The circuit replaces a more costly and bulky push-push mechanical switch. The pushbutton switch triggers a monoshot circuit. The monoshot circuit's output triggers a toggle flip-flop, which inverts its output state and controls power to the load.

Several implementations of the scheme are possible. **Figure 1** shows a single-IC implementation. The circuit uses two flip-flops, IC_1 and IC_2, in the same IC, CD4027B. You configure IC_1 as a monoshot circuit by feeding its output back to its reset pin through an RC network. IC_1 outputs a high on the rising edge of the clock by tying its J input high and its K input low. The pushbutton switch connects between the clock input of IC_1 and ground. The switch can also connect between the clock input and the positive supply, V_{DD}. By tying IC_2's J and K inputs high, IC_2 becomes a toggle flip-flop. The output of IC_1 clocks IC_2 and toggles its output on the rising edge of the IC_1 output.

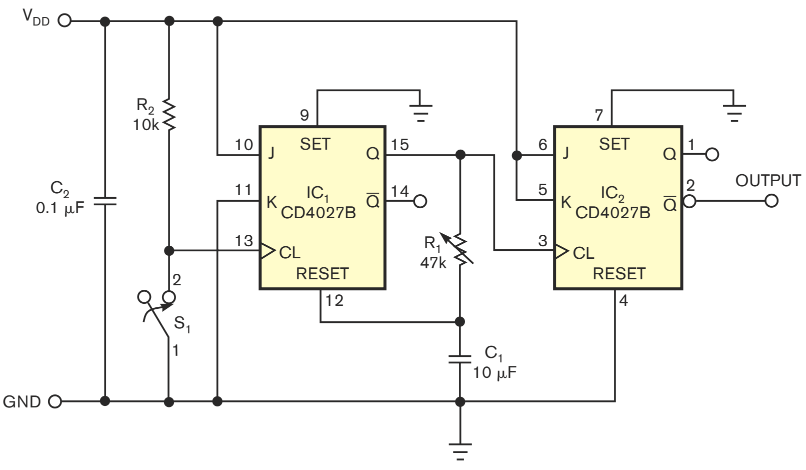

Figure 1 A pair of flip-flops configured as a monoshot and a toggle flip-flop debounce a simple, inexpensive pushbutton switch.

You can understand the operation of the circuit by observing the waveform at different points of the circuit (**Figure 2**). When you press the pushbutton switch, due to debouncing, IC_1's output goes high on the clock's rising edge. Capacitor C_1 starts charging through R_1 toward high voltage. At the same instant, IC_2 receives a rising-edge transition at its clock and toggles its output. When capacitor C_1's voltage exceeds the threshold of the IC_1 reset pin, IC_1 resets, and its output goes low. C_1 now discharges through R_1 to low voltage. The charging and discharging rate of C_1 are equal. The duration of the monoshot circuit's output pulse handles the switch-press time and the debouncing period. Varying

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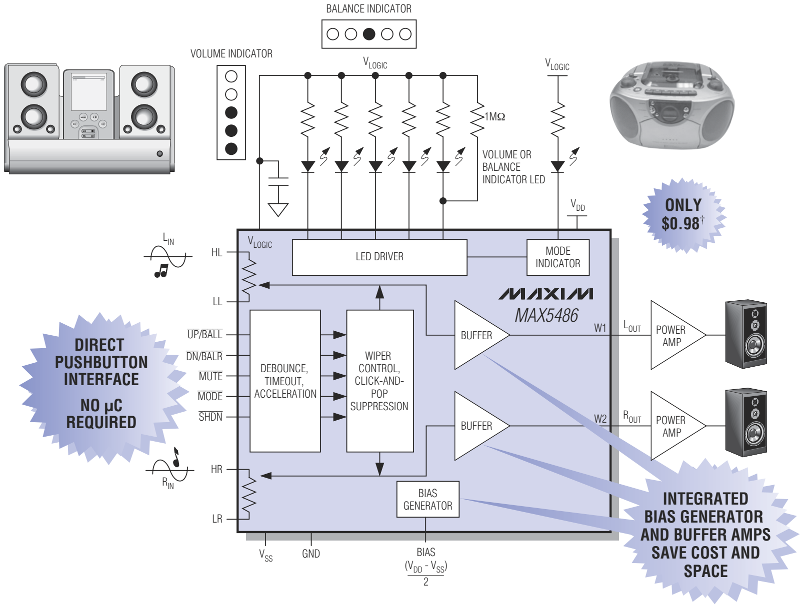

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the value of R_1 varies the pulse period, and you can set R_1 for different types of pushbutton switches. Complementary outputs of IC_2 are available, and you can use them to drive power switches, such as transistors, MOSFETs, relays, and shutdown pins of switching regulators. The circuit operates over a supply voltage of 3 to 15V and can control power to analog and digital circuits.**EDN**

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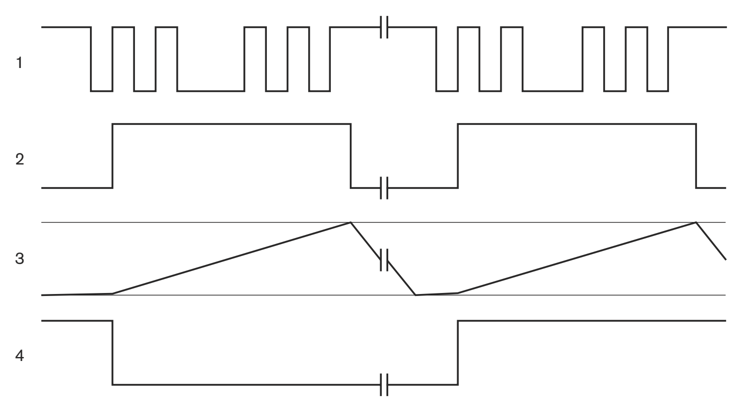

Figure 2 Trace 1 is the voltage across the clock of IC_1, Trace 2 is the output of IC_1, Trace 3 is the voltage on capacitor C_1, and Trace 4 is the output of IC_2.

Microcontroller drives H bridge to power a permanent-magnet dc motor

Luca Bruno, ITIS Hensemberger Monza, Lissone, Italy

A traditional method of driving a low- to medium-power permanent-magnet dc motor involves using four MOSFET or bipolar transistors in an H-bridge configuration. For example, in **Figure 1**, the motor connects between collector pairs C_1 and C_2 and C_3 and C_4. Turning on diagonally opposite transistor pairs Q_1 and Q_3 or Q_2 and Q_4 steers current through the motor and allows for reversal of its direction of rotation. However, this method requires that each of the four transistors receive its own control input. Depending on the motor's voltage requirements, the upper two drive signals may require electrical isolation or a level-shifter circuit to match the microcontroller's output-voltage limitations.

This Design Idea describes an alternative circuit that drives only the H bridge's two low-side switching transistors. In a standard bipolar-transistor H bridge for bidirectional motor control, Q_1's and Q_4's bases connect to Q_3's and Q_2's collectors through resistors R_3 and R_4 (**Figure 2**). Inputs V_{INA} and V_{INB} each control a pair of switches. When Q_2 turns on, resistor R_4 and diode D_6 pull Q_4's base low, saturating Q_4 and pulling current through the motor and Q_2. Similarly, turning on Q_3 pulls Q_1 into saturation and drives the motor in the opposite direction. Diode D_5 ensures that Q_1 remains off when Q_4 conducts, and D_6 performs the same function for Q_4 when Q_1 conducts. Resistors R_1, R_2, R_7, and R_8 increase the switching speed of their associated transistors, and resistors R_5 and R_6 limit base-current drain from the microcontroller's 5V high-logic-level outputs to approximately 15 to 20 mA. Resistors R_3 and R_4 set Q_1's and Q_4's saturation base currents. Their value depends on the motor-supply voltage and Q_1's and Q_4's dc current-gain according to the following equation: $R_3=R_4\le[V_{CC}-V_{BE(ON)}(Q_4)-V_F(D_6)-V_{CE(SAT)}(Q_2)]/[(I_{MOTOR})/$

(continued on pg 82)

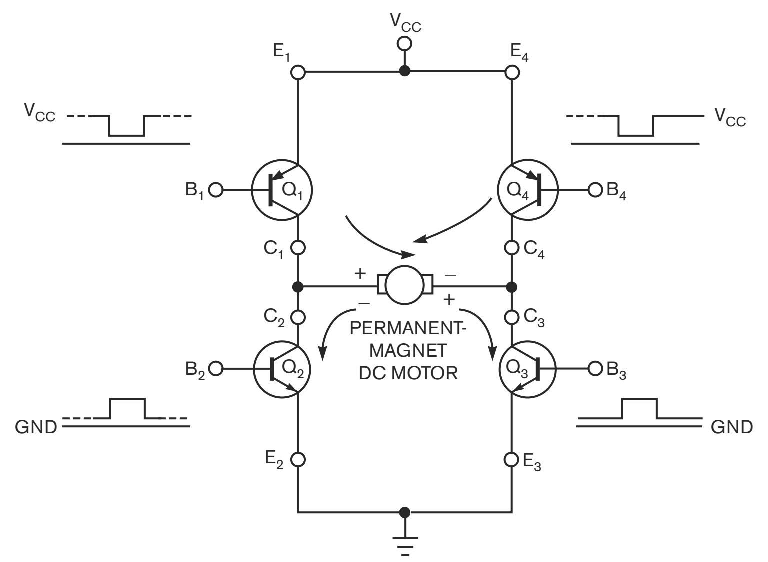

Figure 1 In an H-bridge output-driver stage, diagonally opposed transistor pairs conduct to energize a dc motor. The circuit requires four control signals.

LINEAR TECHNOLOGY

DESIGN NOTES

Simple and Compact 4-Output Point-of-Load DC/DC μModule System – Design Note 411

Jian Yin and Eddie Beville

Introduction

Advancements in board assembly, PCB layout and digital IC integration have produced a new generation of densely populated, high performance systems. The board-mounted, point-of-load (POL) DC/DC power supplies in these systems are subject to the same demanding size, performance and power requirements as other subsystems—demands that are difficult to meet with traditional power modules or controller/regulator ICs. The LTM4601 DC/DC μModule™ converter meets these demands by shrinking an entire solution to the size of a low profile IC. Its frequency synchronization and voltage tracking features allow multiple LTM4601s to be easily and quickly configured for multioutput applications.

4-Output DC/DC Converter Power System

Figure 1 shows the photo of a 4-output DC/DC supply using four μModule converters with frequency synchronization and output tracking. The operating waveforms of the four outputs are interleaved with a 90° relative phase difference, thus reducing the effective input current ripple. This in turn significantly reduces the bulk capacitance of the circuit and the circuit size.

Figure 2 presents the efficiency of each output in Figure 1. With 12V input voltage, each output is tested up to 12A by disabling the other three outputs. The high efficiencies up to 92% guarantee low losses in the circuit board, thus leading to a reduced system profile.

Figure 3 shows the simplified block diagram for Figure 1. For a detailed schematic, please refer to page 22 of the LTM4601 data sheet. An intermediate bus input of 8V–16V is converted to four different outputs: 1.5V at 12A, 1.8V at 12A, 2.5V at 12A and 3.3V at 10A. The output voltages are set by resistances on the LTM4601 VFB pins. A 4-phase oscillator LTC6902 generates 90° interleaved clock signals. Moreover, spread spectrum frequency modulation (SSFM) can be activated by adding an external resistor from the LTC6902 MOD pin to V^+.

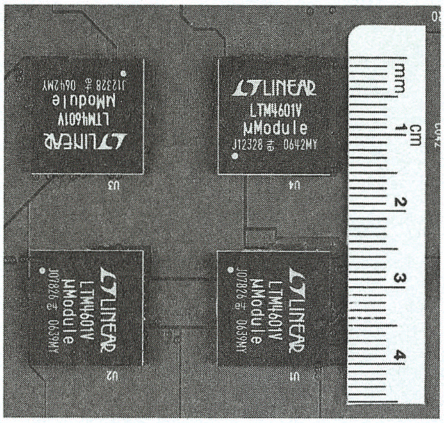

Figure 1. A 4-Output 103W DC/DC System Can Fit This Tiny Space (Each LTM4601 μModule DC/DC Converter Contains an Inductor, MOSFETs, Bypass Capacitors, Etc.)

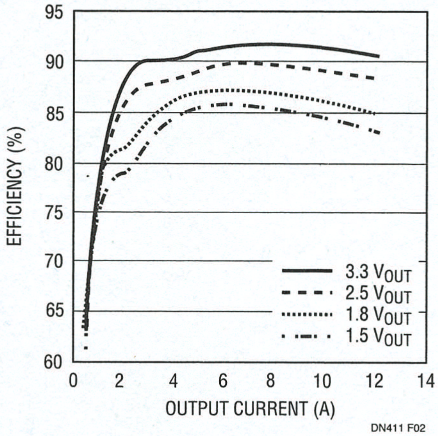

Figure 2. Efficiency of Each Output for the Circuit in Figure 1

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Output Tracking

The output voltage of the LTM4601 can track another converter's output ratiometrically or coincidently. The circuit in Figure 1 implements coincident tracking by connecting the 3.3V output (master) to the TRACK/SS pins of the other µModule converters (slaves) via resistive dividers. For coincident tracking, the master must have a higher output voltage than the slaves. The soft-start capacitor on the TRACK/SS pin of the 3.3V master supply sets the ramp rate of the start-up voltage. Figure 4 shows the start-up waveforms of the four outputs with output tracking.

Frequency Synchronization

The operating frequency of the LTM4601 can be synchronized with an external clock to reduce undesirable frequency harmonics, and its operation can be interleaved with other LTM4601s. Figure 5 shows the input current ripple of the 180° phase-interleaved 1.8V and 3.3V outputs of the circuit in Figure 1. The input current ripple of the 3.3V output is synchronized with its PLLN signal in Figure 5. Therefore, with four 90° interleaved inputs, the input current ripples are partially cancelled, reducing the required input capacitance.

Conclusions

The synchronization and tracking features of the LTM4601 allow interleaved phases in the 4-output solution, thus reducing input capacitance and producing a compact design. High efficiency and excellent thermal performance make it possible to handle the total maximum power of 103W in a 4-layer PCB at 11cm × 11cm.

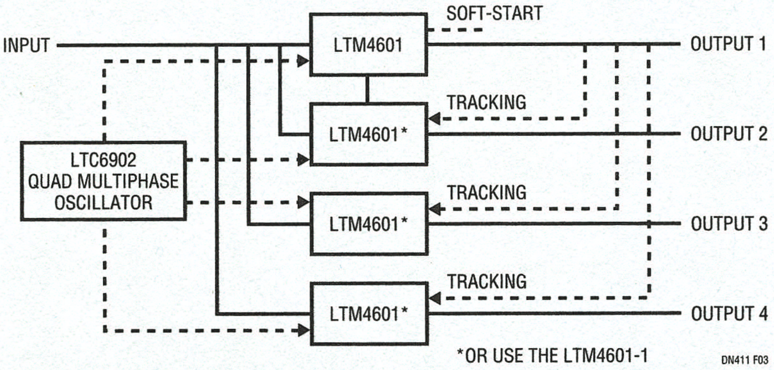

Figure 3. Simplified Schematic of a Compact 4-Output Point-of-Load DC/DC µModule Converter Solution. The LTC6902 Interleaves the Operating Waveforms of the Four µModule Converters, So That the Ripple Currents Cancel Each Other. This Significantly Reduces the Size of the Required Input Capacitors. Start-Up and Shutdown Voltage Rracking Is Simply Accomplished by Connecting the Output of the 3.3V µModule (Output 1) to the Other µModule Converters

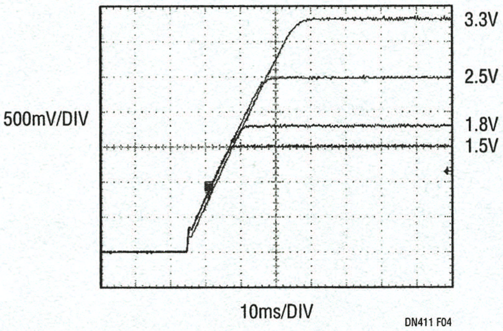

Figure 4. Start-Up Voltage Waveforms of the Circuit in Figure 1 Show Coincident Tracking of the Outputs

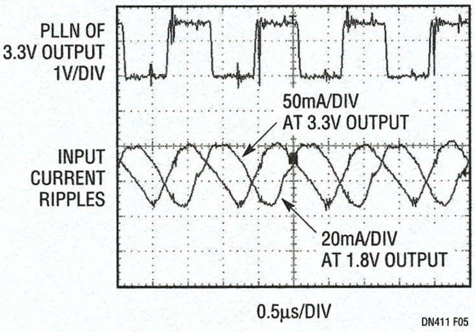

Figure 5. Input Current Ripple Is Reduced by Interleaving the Operation of the Supplies Using Frequency Synchronization

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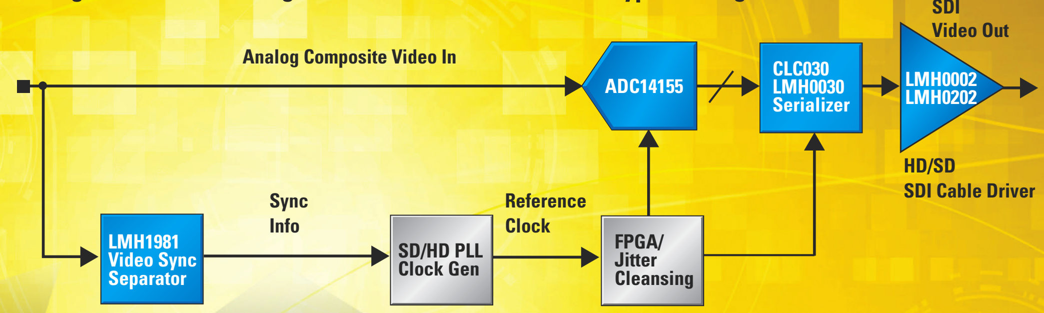

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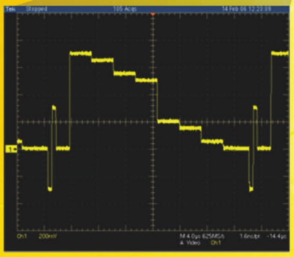
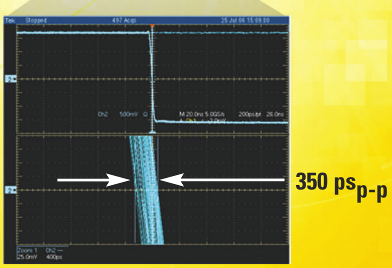


720p/60 Tri-Level Input



720p/60 H-Sync Output

LMH1981 in TSSOP-14 packaging
Shown at actual size 4.40 x 5.00 x 0.90 mm

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LEAD-FREE

LMH1981 Features

- 50% sync slicing
- Low-jitter horizontal sync outputs
- Supports NTSC, PAL, SECAM, 480i, 480p, 576i, 576p, 720p, 1080i, and 1080p
- Accepts video sync signals from 140 mV$_{P\text{-}P}$ to 1.2 V$_{P\text{-}P}$
- No external programming with µC required
- Horizontal sync output propagation delay <50 ns
- 3.3V or 5V single supply operation

LMH1981 Outputs

- Horizontal sync
- Vertical sync
- Odd/Even field
- Burst/back porch clamp
- Composite sync
- Video format (horizontal lines/field)

Ideal for use in sync separation, A/V clock generation, video genlock, back porch clamp generator, video format detection circuit, and analog-to-SDI converter applications

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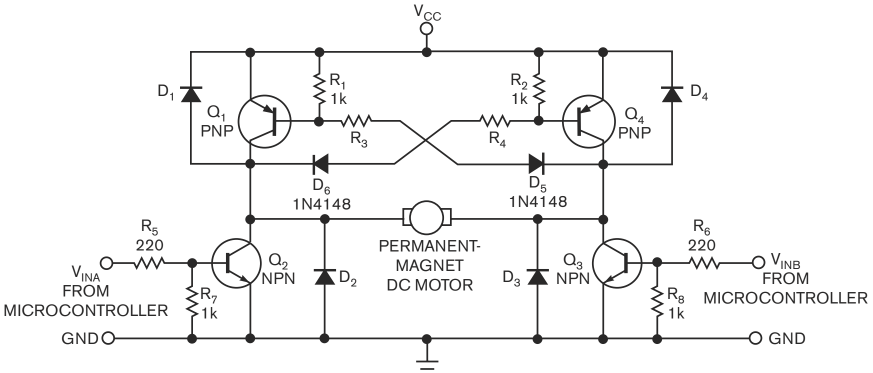
Or call 1-800-272-9959

National Semiconductor
The Sight & Sound of Information

(continued from pg 78)

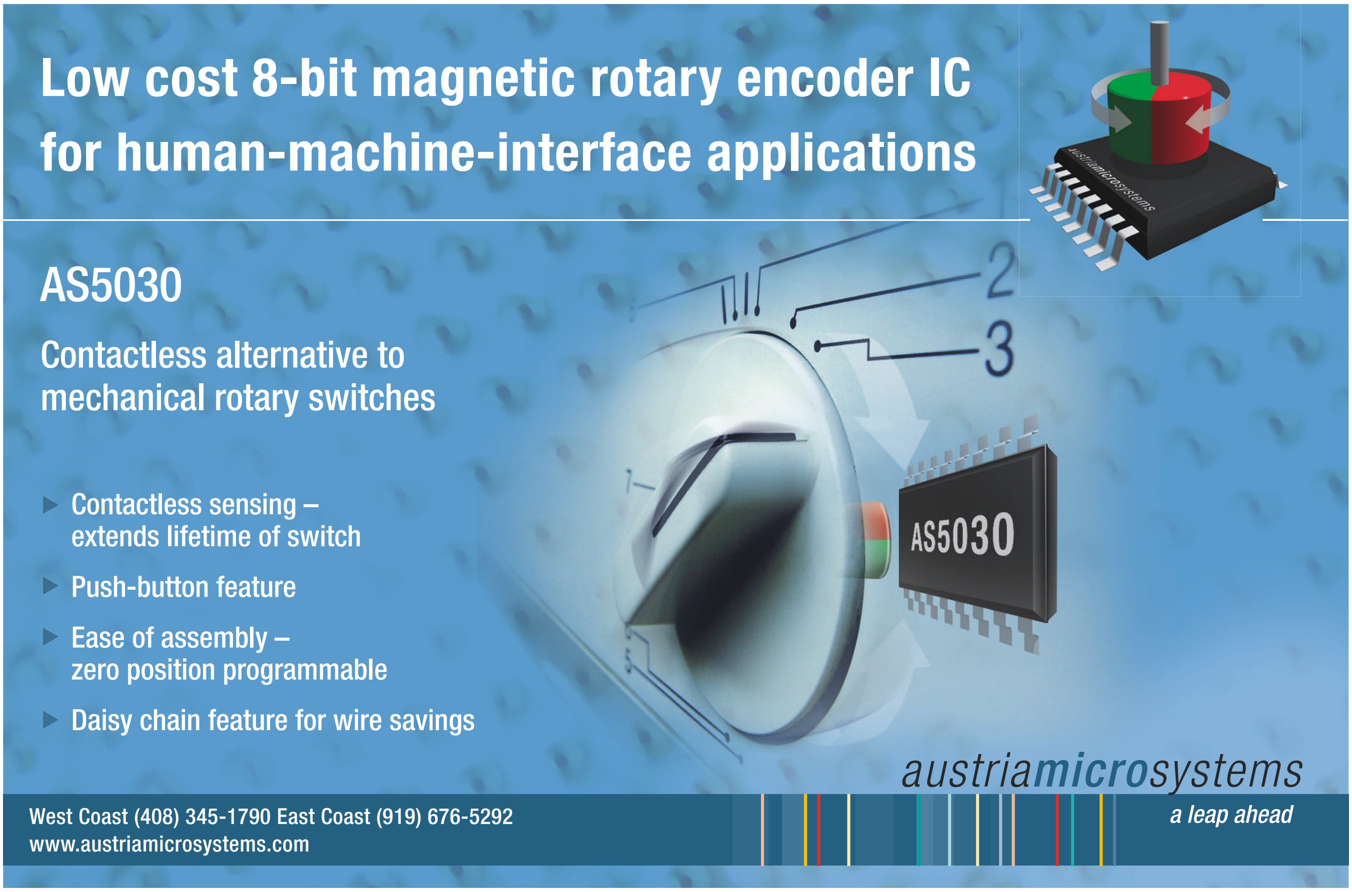
$h_{FE(MIN)}(Q_4)$]. For best performance, select bipolar-junction transistors with low collector-emitter saturation voltages, $V_{CE(SAT)}$, and high values of dc-current gain, h_{FE}. Currently available medium-power transistors compete favorably with MOSFETs by offering these characteristics in combinations that minimize collector-power dissipation and require little base drive.

Discrete devices such as On Semiconductor's (www.onsemi.com) NSS40200LT1G PNP and NST489AMT1 NPN bipolar transistors work well in the circuit in **Figure 1**. For a more compact implementation, you can select an integrated H bridge, such as Zetex's (www.zetex.com) ZHB6790, which operates at power-supply voltages as high as 40V, with 2A continuous and 6A peak pulse-current collector ratings. Its minimum current gain of 500 at a collector current, I_C, of 100 mA can decrease to 150 at I_C of 2A. At a worst-case collector current of 2A in Q_2 and Q_3, achieving a saturation voltage of 0.35V or less requires a base current of 13 to 20 mA. Fortunately, many microcontrollers' outputs can source or sink as much as 25 mA and thus directly drive the H bridge independently of the motor's power-supply voltage. To further reduce drive current or to use a standard CMOS or TTL IC as a drive source, you can buffer Q_2's and Q_3's inputs with small-signal transistor inverters. As an option, you can connect fractional-ohm resistors between the emitters of Q_2 and Q_3 and ground. This approach can provide analog voltages proportional to motor current, allowing the microcontroller to detect a stalled or overloaded motor.**EDN**



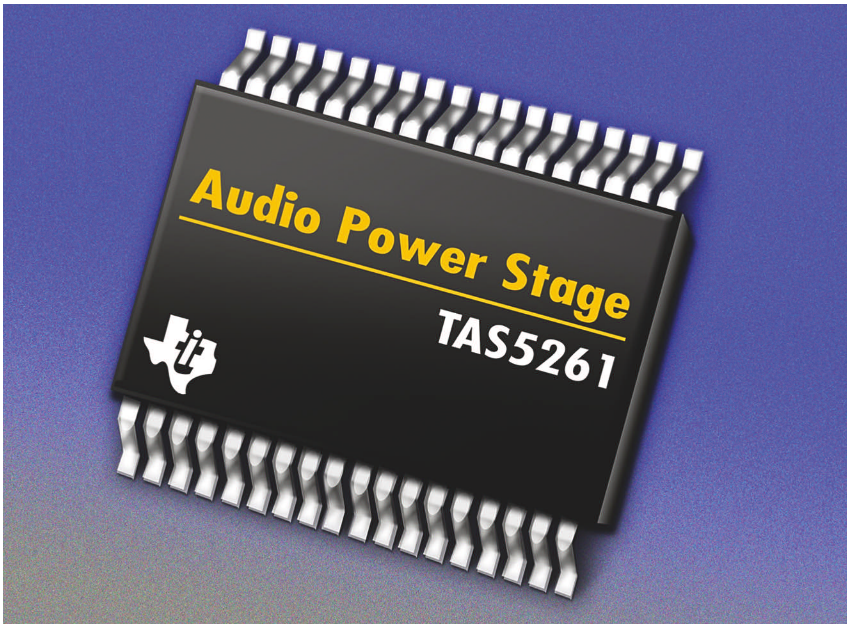
NOTES:
D_1, D_2, D_3, AND D_4 ARE UF5401 ULTRAFAST RECTIFIER DIODES.
SEE TEXT FOR VALUES OF (VISHAY) R_3 AND R_4.
SEE TEXT FOR PART NUMBERS OF Q_1 THROUGH Q_4.

Figure 2 This improved H-bridge-driver circuit uses transistors in complementary pairs and requires only two low-level control signals.



productroundup

AMPLIFIERS, OSCILLATORS, AND MIXERS



Digital-audio amplifier drives 300W on one channel

Claiming efficiency greater than 95%, the TAS5261 digital-audio amplifiers provide a 110-dB SNR. The single-chip device drives 300W into a 4Ω speaker. The PurePath Digital power stage features a 0.09% THD+N (total-harmonic distortion plus noise) at 8Ω. The amplifier eliminates the need for discrete components, such as MOSFET H bridges. Available in a PSOP-3 package, the 300W TAS5261 costs $5.25 (1000).

Texas Instruments, **www.ti.com**

Custom-lowpass/rise-time filters have absorptive design

Users can build the PSPL Model 5915 filters to a −3-dB cutoff frequency ranging from 35 MHz to 10 GHz and a 10 to 90% rise time of 35 psec to 10 nsec. An absorptive design provides attenuation and group-delay characteristics similar to fourth-order Bessel-Thompson filters, claiming a superior transient response. The design provides a high-impedance match in and above the filter passband. Additional features include a −15-dB typical return loss and a 0.02-dB insertion loss at dc. The filters provide compatibility with various standards and data rates, including SONET (synchronous optical networking), SDH (synchronous digital hierarchy), Gigabit Ethernet, PCIe (PCI Express), SATA (Serial Advanced Technology Attachment), and HDMI (High Definition Multimedia Interface). Available in a five-day turnaround time, the PSPL Model 5915 costs $495.

Picosecond Pulse Labs, **www.picosecond.com**

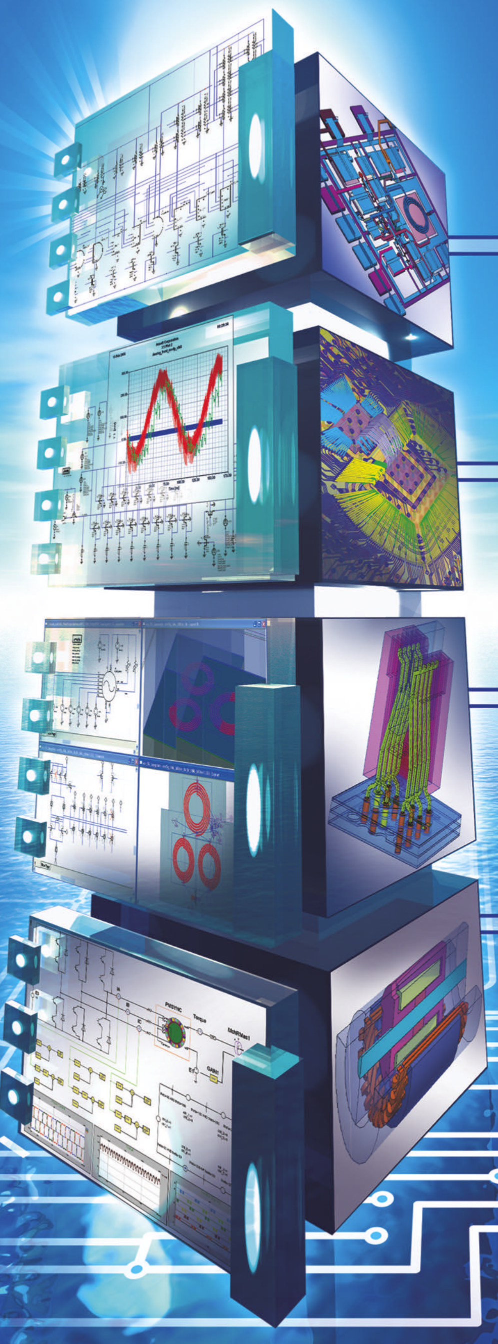
ADC drivers provide low distortion

Enabling a dc to 100-MHz performance, the ADA4937-1 and ADA4938-1 ADC drivers target data-acquisition systems and wireless-infrastructure equipment. Suiting 3 to 5V power supplies, the ADA4937-1 features −120/−102-dBc distortion at 10 MHz, −98/−100-dBc distortion at 40 MHz, and −84/−90-dBc distortion at 70 MHz. Targeting use with 5 to 10V power supplies, the ADA4938-1 provides −112/−108-dBc distortion at 10 MHz, −96/−93-dBc distortion at 30 MHz, and −79/−81-dBc distortion at 50 MHz in dual-supply applications. The vendor's specialized XFCB-3 SiGe (silicon-germanium) SOI (silicon-on-insulator) technology allows the low distortion. The ADA4937-1 provides 16-bit performance at 40 MHz, 14 bits at 70 MHz, and 12 bits at 100 MHz. Measuring 3×3 mm, the device also provides an internal common-mode-feedback architecture. Available in an LFCSP (lead-frame chip-scale package), the ADA4937-1 and ADA4938-1 cost $3.79 (1000).

Analog Devices, **www.analog.com**

Bus-controlled audio-power amplifier targets mobile phones

Aiming at mobile phones, the compact, three-output TS4956 bus-controlled audio-power amplifier includes an I^2C interface, providing eight operating modes, including a stereo-loudspeaker option and a 32-step, −34- to +12-dB digital-volume control. Features include 0.5-µA standby current; 10-nA shutdown current; the ability to operate on a 2.7 to 5.5V power supply; and pop-and-click noise-reduction circuitry, eliminating turn-on and turn-off noise. The device monitors the output voltage and current in the phantom-ground configuration, limiting the headphones' power output and minimizing the chance of hearing damage. The amplifier can drive 38 mW per chan-



AMPLIFIERS, OSCILLATORS, AND MIXERS

nel of continuous average power in 16Ω headphone loads or 450 mW into 8Ω loudspeaker loads when operating on a 3.3V power supply. The device provides an overtemperature-shutdown mechanism activating at 150°C, with a −40 to +85°C temperature range. Available in a lead-free, 2.5×2.4-mm, 18-bump flip-chip package, the TS4956 costs $1.10 (1000).

STMicroelectronics, www.st.com

Fuel gauge reports battery capacity without a full-charge cycle

Using a combination of an OCV (open-circuit-voltage) battery model and coulomb counting, the standalone DS2786 OCV-based fuel gauge estimates the available capacity of rechargeable lithium-ion batteries. The device provides accurate capacity information immediately after a user connects a battery pack to the host. During moderate- to high-discharge rates, the fuel gauge uses coulomb counting as a secondary method of estimating relative capacity. Able to detect pack capacity from a partial-charge or -discharge cycle, this feature eliminates the need for a full-charge or -discharge cycle. Features include a 12-bit voltage measurement with ±10-mV accuracy and 1.22-mV resolution; a bidirectionally measured current with 11-bit resolution; and two auxiliary voltage inputs aiming at measuring resistor ratios, suiting thermistor or pack-identification-resistor measurement. Additional features include an I^2C interface and an OCV-look-up table and other parameters stored in 32 bytes of on-chip EEPROM. Internal measurements provide ±3°C accuracy. Measuring 3×3 mm in a TDFN-10 package, the DS2786 costs $1.22 (10,000).

Dallas Semiconductor, www.maxim-ic.com

EMBEDDED SYSTEMS

Small modern module features an RJ-11 connector

Measuring 0.66×1.25×0.75 in., the TinyModem modern module has an RJ-11 connector. The device's self-contained TTL interface tolerates 3750V of isolation voltage. Features include caller ID, line-in-use detection, extensive pickup, call waiting, remote hang-up detection, voice playback, and recording capability. In addition, the device provides 56- to 300-kbps data rates and a 14.4-kbps fax rate. The TinyModem costs $29 (1000).

Radicom Research, www.radi.com

Dual-channel ADC provides front-end processing

Based on Xilinx's Virtex-5 LX110 FPGA-based PMC module with two integrated analog-input channels, the PMC-FPGA05-ADC1 provides front-end processing by combining a dual analog interface with the processing power and PCI-X bus interface. Features include three QDRII SRAM banks with 8 Mbytes per bank, two DDR2 SDRAM banks with 128 Mbytes per bank, and a Xilinx VC5VLX110 Virtex-5 FPGA. Providing interfaces from the FPGA, the module supports a 133-MHz PCI-X interface and a PMC digital-user I/O through the Pn4 connector. The PMC-FPGA05-ADC1 costs $7995.

Vmetro, www.vmetro.com

Embedded-networking module enables drop-in network connectivity

The XPort Direct embedded-networking gateway suits applications moving commands, status, and information over IP (Internet Protocol) networks or the Internet to or from remote devices. Mounted on a PCB (printed-circuit board), the module enables drop-in network connectivity. This feature allows OEMs to differentiate their products by providing a range of capabilities, including remote diagnostics, monitoring, maintenance, and control. The XPort Direct module costs $20.

Lantronix, www.lantronix.com

Data-acquisition cards provide high throughput

Available in PCI and PXI form factors, the DAQ-2016 and PXI-2016 data-acquisition cards suit large-scale data collection and industrial automation. Features include an 800k-sample/sec/channel maximum-transfer rate; two 12-bit, 1M-sample/sec, analog-output, 24-channel, programmable digital I/Os; and two 16-bit timer/counters, providing flexibility for multitasking situations. In addition, the device includes a WDM (Windows-driver-model) driver for C/C++, Virtual Basic, Delphi, C++ builder, and .NET programming languages and the Matlab and LabView device drivers. The DAQ-2016 and PXI-2016 cards cost $1495 and $1695, respectively.

Adlink Technology, www.adlinktech.com

productroundup

EMBEDDED SYSTEMS

Development environment suits real-time applications

Suiting Java developers creating resource-constrained and deeply embedded hard-real-time applications and components, the PERC Pico development environment claims similar execution speed to C/C++ programs and a three-times increase in speed compared with Java programs. Features include deterministic response times of microseconds, the ability to directly access low-level hardware devices, and a 256-kbyte memory footprint. Available for Linux/x86 platforms, the development environment is portable to major processor architectures for RTOS and bare-board platforms. PERC Pico development tools cost $25,000 for an unlimited number of developers.

Aonix, www.aonix.com

INTEGRATED CIRCUITS

Integrated AM/FM-radio receiver combines antenna input, audio output

Integrating an antenna input and an audio output in a monolithic IC, the Si473x AM/FM-radio-receiver family requires no manual alignment. Requiring two external components in a 0.15×0.15-cm board, the digital architecture supports a variety of antennas with an on-chip varactor and autocalibration. Features include high sensitivity and selectivity, an adjustable soft mute, and support for the European RDS (Radio Data System) and the US RBDS (Radio Broadcast Data System), enabling the display of station ID and song name. Available in a 3×3-mm QFN-20 package, the Si4731 costs $5.53 (10,000), and an evaluation board is available for $150.

Silicon Labs, www.silabs.com

Active HDMI switches meet the 1.3-HDMI standard

The PI3HDMI341xxx, PI3HDMI412AD, PI3HDMI421AR, and PI3HDMI411AD active HDMI (High Definition Multimedia Interface) switches provide compliance with the 1.3-HDMI standard. The active 1-to-1, 2-to-1, 3-to-1, or 1-to-2 multiplexer/demultiplexer switches operate at 2.5 Gbps with 12-bit/channel deep-color support. The lead-free devices provide 1080p high-resolution-video support with 12-bit-color depth per channel. Available in TQFN-56 or LQFP-80 packaging, the active HDMI switches sell for $1.50 to $3 (10,000).

Pericom Semiconductor, www.pericom.com

Multichannel DACs integrate a variety of features

Suiting factory-process control, instrumentation, and dc setpoint-control applications, these 16-bit DACs integrate output amplifiers, references, and a diagnostic feature. The multichannel AD5754 and AD5754R DACs include 12 converters ranging from 12- to 16-bit dual- and quad-channel devices operating on either single or dual power supplies. Features include software-programmable, unipolar and bipolar voltage-output ranges, which you independently set for each channel, and the vendor's iCMOS industrial-manufacturing process. The monotonic AD5754R provides a 0.1% maximum accuracy level and includes a precision 5-ppm/°C internal reference. Available in TSSOP packaging, the 16-bit AD5754 and AD5754R quad devices cost $10.05.

Analog Devices, www.analog.com

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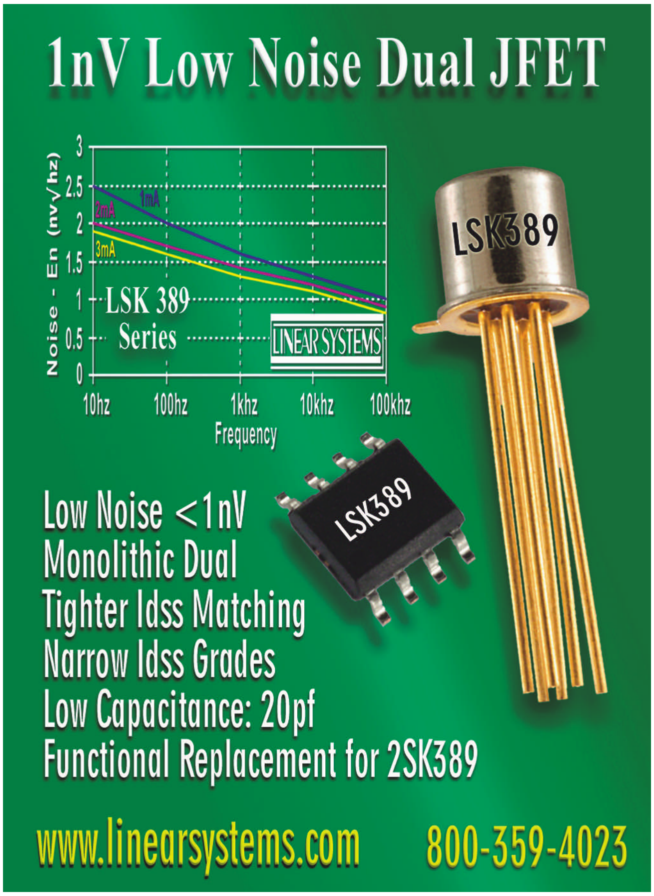

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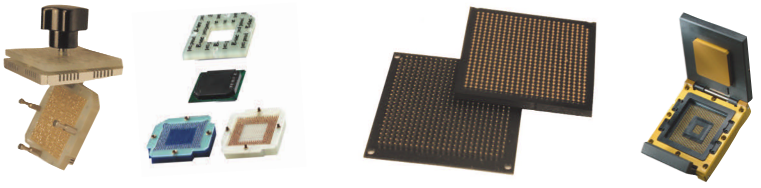

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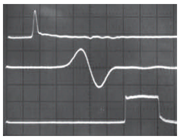
PULSE GENERATORS AND ACCESSORIES



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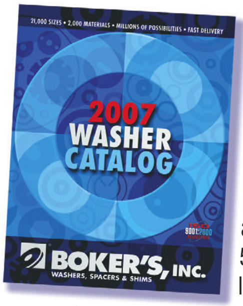

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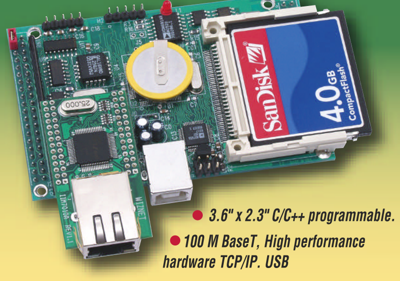

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scope

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LOOKING AHEAD

TO *EDN*'S INNOVATION AWARDS ANNOUNCEMENT

The nominations are in, the judges have selected the finalists, and eager voters flocked to pick their favorites for the 17th annual *EDN* Innovation Awards. Everything leads to the announcement of the winners at our awards ceremony in San Jose, CA, on the evening of April 2. Then, the April 12, 2007, edition of *EDN* will spotlight the winners. The awards recognize remarkable achievements in electronics-design engineering and are worth watching on that basis alone. But they also give a sense of where the best minds are taking electronics technology—a quick summary of the trends that will play out in the design lab and the marketplace in the next few years. For more information, visit www.edn.com/innovation.

LOOKING BACK

TO THE BEGINNINGS OF HANDHELD VIDEOCAMERAS

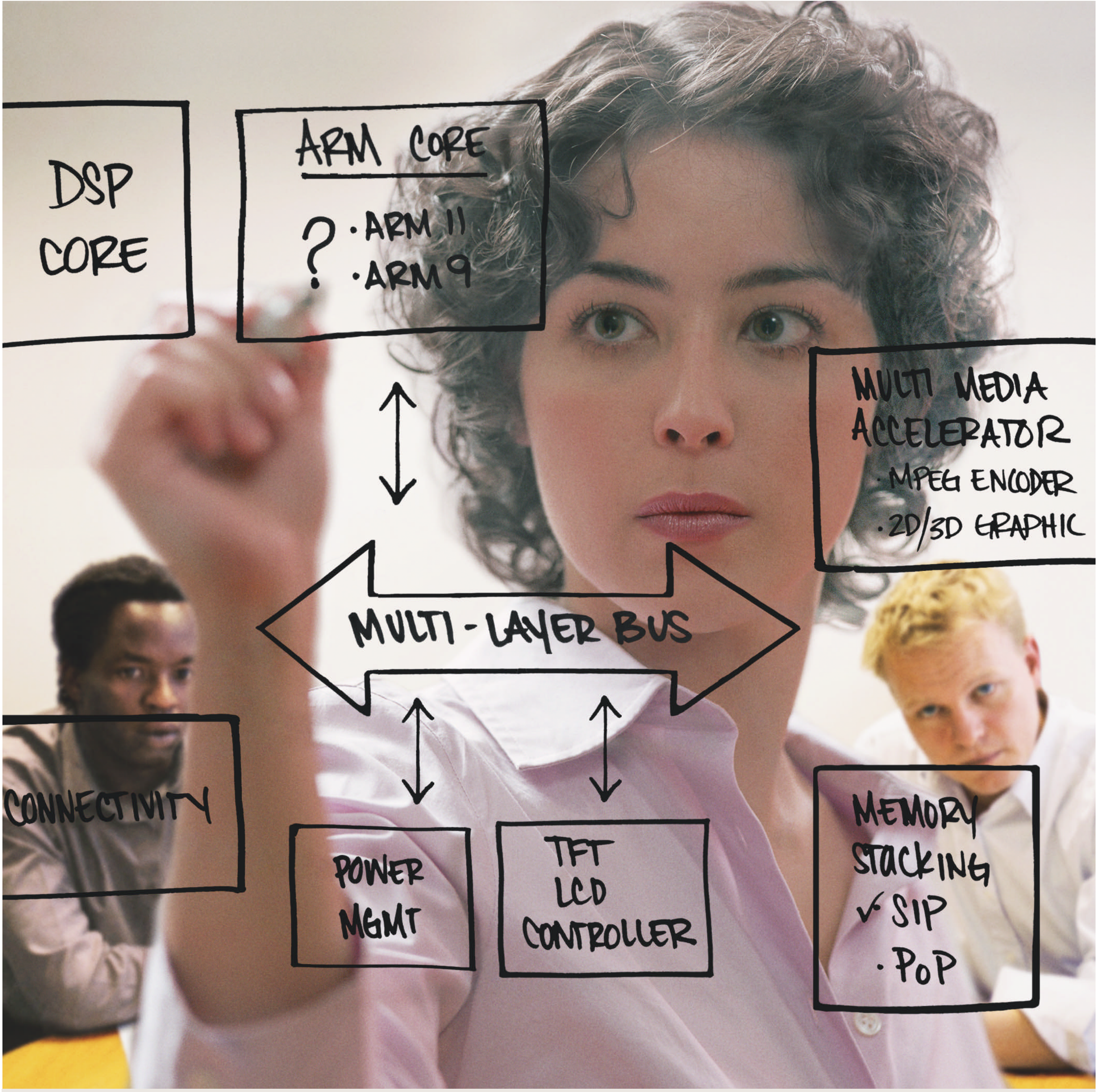
A pocket-sized TV camera, which weighs less than a pound, surpasses standard vidicon-type industrial cameras in sensitivity, according to developers at RCA. RCA engineers combined transistors with a new half-inch vidicon tube in the design. The first such camera to employ photoelectric iris control, the device accommodates scene-lighting changes on the order of 100-to-one. With its f/1.9 lens, the camera requires only 10 foot candles of scene illumination to transmit clear pictures with good contrast. It measures 1.9×2.4×4.5 inches and may be operated in the hand, on a tripod, or bolted to a wall or floor. RCA intends the camera for military airborne, mobile, and field closed-circuit operation.

—*Electrical Design News*, March 1957

LOOKING AROUND

AT GROWING IC-PROCESS FRAGMENTATION

Advanced semiconductor processes—excluding specialty items, such as DRAM and RF—at one time appeared to be converging on almost a single formula. Fab-equipment sets, the way process engineers employed the equipment, and even process controls were similar. The result was that the choice of a foundry had little impact on chip architecture or circuit design in the digital domain. But those days may be departing. Foundries appear to be clumping into groups—such as the Common Platform Alliance comprising IBM, Chartered Semiconductor, Samsung, and Infineon—to share process-development costs. But the clusters appear to be moving away from each other—employing immersion lithography at different layers, taking different approaches to adaptive process controls, and preparing mask data with different tools. All these issues can affect what works and what doesn't in a design, even at the architectural level. This issue may not be big at the 65-nm process, but, by 45 nm, it could mean that the choice of foundry will make important differences all during the chip-design process.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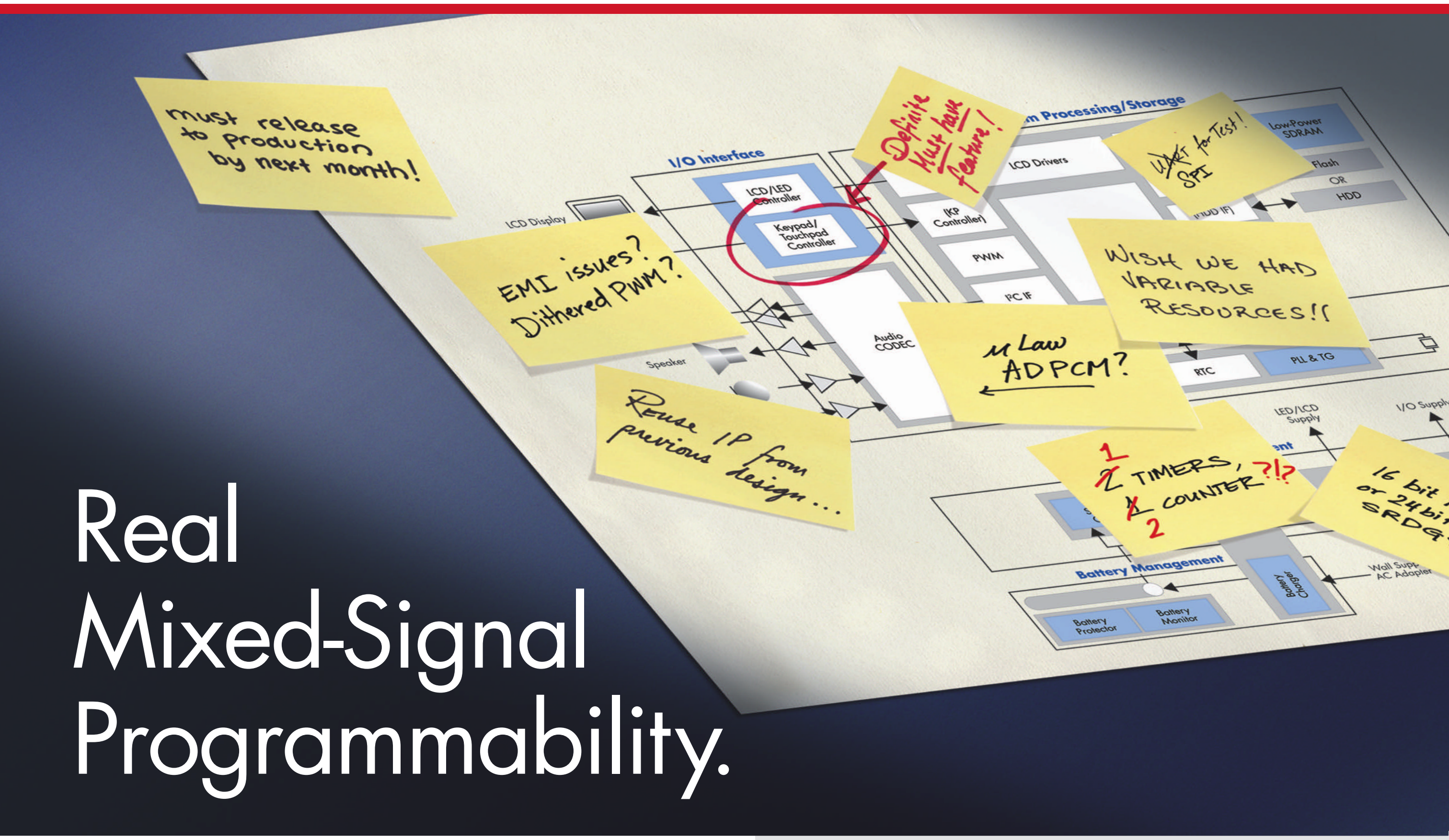

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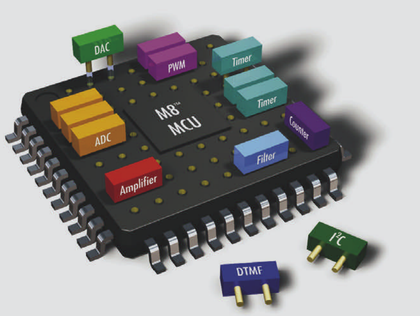

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